A Highly Linear and Low Flicker-Noise CMOS Direct Conversion Receiver Front-end for Multiband Applications

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A Highly Linear and Low Flicker-Noise CMOS Direct Conversion Receiver Front-end for Multiband Applications

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Summary

This dissertation focuses on design and implementation of a highly linear and low flicker-noise receiver front-end based on the direct conversion architecture for multiband applications in a CMOS technology. The dissertation consists of two parts: One, implementation of a highly linear RF receiver front-end for multiband applications and, two, implementation of a low flicker-noise RF receiver front-end based for direct conversion architecture. For multiband applications, key active components, highly linear LNAs and mixers, in the RF front-end receiver have been implemented in a 0.18um CMOS process. Theoretical approaches are analyzed from the perspective of implementation issues for highly linear receiver system and are also compared with measured results. Highly linear LNAs and mixers have been analyzed in terms of noise, linearity and power consumption, etc.

For a low flicker-noise receiver front-end based on direct conversion architecture, the design of differential LNA and various low flicker-noise mixers are investigated in a standard 0.18um CMOS process. Device measurements and theoretical analyses were implemented to optimize the design of a low flicker-noise receiver front-end. A differential LNA which shows high linearity was fabricated with a low flicker-noise mixer. Three low flicker-noise mixers were designed, measured and compared to the-state-of-the-arts published by other research institutes and companies. Also, simulation results for a harmonic-tuned VCO to improve the flicker noise performance of receiver front-end have been shown.

CHAPTER I

Introduction

1.1 Technology trends

The superheterodyne architectures have shown superior performances in terms of receiver's selectivity and sensitivity as compared to the direct conversion architectures because they use more filtering stages at the intermediate frequency (IF) stage [1]. However, as the demands for low cost and low power solutions are increased in the wireless market, it has been shown that the direct conversion architectures are the better choices for low cost and low power wireless applications. In a direct conversion receiver, the RF signal is down-converted to DC directly, which eliminates the need for expensive off-chip filtering and image frequency issues. Even if direct conversion architectures are extremely attractive to realize highly integrated solutions for wireless applications, they have a few drawbacks: flicker noise, dc offset, even-order distortion, local-oscillator (LO) pulling, and LO leakage [2]. Flicker noise degrades the signal-to-noise ratio (SNR) and total noise figure, which results in the degradation of receiver sensitivity. CMOS transistors suffer from high intrinsic flicker noise, which is inversely proportional to the WL of the device [3]. Therefore, minimum length of the device increases flicker noise. In general, a mixer is the main source of flicker noise generation in CMOS receivers. Passive CMOS mixers are considered as the appropriate choice for direct conversion receivers because they do not contribute to flicker noise. However, due to conversion loss, a higher gain of LNA is required to minimize baseband noise contribution. In order to

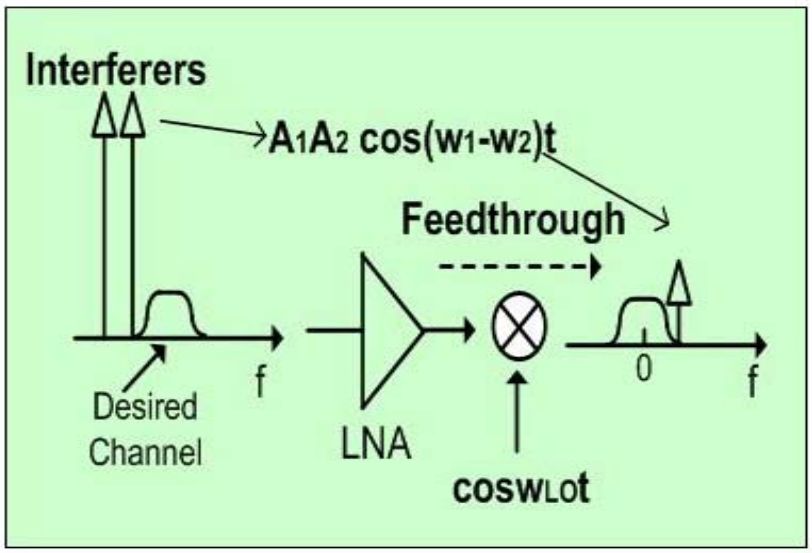
decrease flicker noise in CMOS active mixers, the bias current of the LO switches should be small enough to lower the height of noise pulses. The static current bleeding technique was proposed to reduce the bias current of the LO switches [4]. Also, the tail capacitance should be minimized to decrease the indirectly translated flicker noise [5].

Another issue discussed in this thesis on multiband direct conversion receivers is linearity issue. Linearity is one of key issues in multiband RF systems because nonlinearity in RF systems for multiband applications causes many problems, such as gain compression, desensitization, cross modulation, and intermodulation, etc. To implement a highly linear receiver, low-noise amplifier (LNA) and mixer should be designed with very high linearity. Several linearization techniques for CMOS LNAs have been proposed so far by various research institutes. Comparing to CMOS LNAs, less linearization techniques have been proposed for CMOS mixers because mixers show complicated nonlinear phenomenon. To make a highly linear and low flicker-noise mixer, the derivative superposition (DS) method should be applied to the RF transconductance stage of a Gilbert-type mixer with resonating technique, which results in improved linearity and flicker noise performance simultaneously.

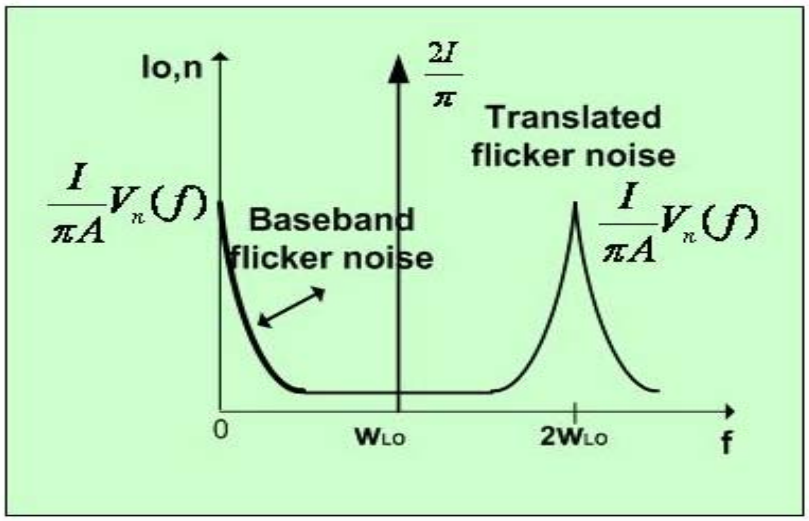
1.2 Motivation for dissertations

In general, typical RF receivers suffer from only odd-order intermodulation. On the other hand, even-order distortion can be a critical issue in direct conversion receivers [2]. As shown in Figure 1.1(a), a low-frequency beat in the presence of even-order distortion is generated by two high-frequency interferers. When the two-tone signals are

applied to the nonlinear circuit, undesirable baseband spectral component, $A_1 A_2 \cos(\omega_1 - \omega_2)t$, is generated. This spectral component degrades the reception quality of the desired signal. Usually, the downconverter determines the achievable second-order input intercept point (IIP2) of the receiver.



(a)



(b)

Figure 1.1 (a) Effect of even-order distortion on interferers (b) Mixer output spectrum in presence of flicker noise

Another important drawback of direct conversion architecture in a CMOS technology is flicker noise because the signal downconverts to baseband after only minimal amplification with LNA. Therefore, a mixer is the main source of flicker noise generation in a direct conversion receiver whose flicker noise tends to limit the receiver's signal to noise ratio (SNR). As can be seen from Figure 1.1(b), flicker noise in the RF transconductance stage is upconverted to ω_{LO} and to its odd harmonics, while white noise at ω_{LO} is translated to DC. On the other hand, low-frequency noise at the gate of the LO switch appears at the mixer output without frequency translation [5]. Therefore, flicker noise around DC should be minimized to utilize as many channels as possible around DC in modern wireless communication systems which use direct conversion architectures.

A critical challenge in the implementation of a highly linear and low flicker-noise receiver is to realize a highly linear mixer with a LNA which has a high third-order input intercept point (IIP3) and simultaneously to design a low flicker- noise mixer to meet the stringent specifications. This will be followed by a survey on the advantages and drawbacks of the techniques that are currently used to realize a highly linear and low flicker-noise receiver front-end.

1.3 Organization of dissertation

This dissertation consists of two contributions. First, a highly linear CMOS receiver front-end implementation for the multiband direct conversion architectures including highly linear LNAs and mixers will be discussed, and the measured results will be demonstrated. Second, a low flicker-noise CMOS receiver front-end for direct conversion architecture will be presented. Chapter Two provides an overview of the

highly linear receiver front-end. In this chapter, fundamental theories to implement a highly linear receiver front-end are discussed. The previous approaches to realize highly linear LNAs and mixers by other research institutes are illustrated and reviewed from the perspective of implementation issues. Chapter Three provides an overview of the low flicker-noise receiver front-end implementation using CMOS technology for direct conversion architectures. The theoretical and technical backgrounds on flicker noise generated by CMOS device have been surveyed and also the flicker noise mechanism caused by a direct conversion receiver front-end has been studied. In addition, some examples of low flicker-noise CMOS mixers published by other research institutes are shown and compared. Chapter Four presents design of a highly linear receiver front-end for multiband application in a 0.18um CMOS process based on the implementation of a highly linear LNA directly connected to a highly linear mixer. Various techniques to design highly linear CMOS LNA and mixers are reviewed in conjunction with the issues of the implementation of a highly linear direct conversion receiver front-end for multiband application. Also, the simulated results of LNAs and mixers are shown and compared with the measured results. Chapter Five shows design of a low flicker-noise direct conversion CMOS receiver front-end. In this chapter, flicker noise mechanisms and design methodologies for low flicker-noise CMOS mixers are mainly discussed and shown. Various experimental results acquired by fabricated 0.18 um CMOS mixers are shown and compared with the simulated results. Also, these measured results have been compared with state-of-the-arts published by other research institutes and companies. In addition, design considerations with simulated results from voltage-controlled oscillator (VCO) perspective are discussed and explained to improve the flicker noise performace

of receiver. Finally, Chapter Six concludes the dissertation with a discussion on potential future work. Future work includes more linearization techniques in receivers for multiband application and some known problems in direct conversion receivers like dc-offset and I/Q imbalance.

CHAPTER II

Highly Linear Receiver Front-end

Linearity, power, noise, and gain are important design issues in the multiband applications for modern wireless receivers. As the RF systems evolve, more demands for multiband functions are required. Therefore, the linearity of a receiver front-end will be one of key issues for reliable RF systems. The required receiver linearity is affected by two main factors. First, the receiver should protect against intermodulations among strong adjacent channels. This means that the third-order input-referred intercept point (IIP3) of the receiver must be higher enough to withstand this effect. Second, some portions of the transmitted signal leak into the receiver and appear as a blocker because no perfect duplexer exists. If the IIP3 of the receiver is greater than a certain power level, then any leaked signal and out-of-band blockers will not force the receiver to be into compression [44, 45].

2.1 Highly linear Low-Noise Amplifier (LNA)

To implement a highly linear receiver front-end, a highly linear low-noise amplifier (LNA) should be implemented in combination of with a low noise figure (NF), high gain, and low power consumption. In fact, the high linearity of LNA has been necessarily required for code-division multiple-access (CDMA) specification which has

the single tone desentization requirement. To meet the specification, the cross-modulation distortion of a single-tone jammer in the presence of a transmitted signal leakage should be reduced [6]. Up to now, several linearization techniques to improve of IIP3 of RF amplifiers or LNA have been implemented. Some of them are based on negative feedback circuits. One of the most demanding techniques is based on series feedback using source degeneration by resistors or inductor [46]. Source degeneration method using an inductor is quite attractive because it does not degrade the noise performance. The cascaded parallel feedback technique was proposed in [47] and this method has a gain reduction problem. By using a simple technique based on low-frequency low-impedance base termination for a Si bipolar junction transistor or a SiGe HBT, the linearity performance was improved as shown in [16], and also a feed-forward distortion cancellation technique was proposed to make a high linear CMOS LNA [17].

2.1.1. linearization using optimum gate biasing

An efficient linearization technique for an FET was proposed by biasing at a gate-source voltage (V_{GS}) at which the third-order derivative of its dc transfer characteristic is zero [18,40,48,49]. The small-signal output current of a common-source FET can be expressed by the following power series in terms of the small-signal gate-source voltage around the bias point

$$i_d(v_{gs}) = g_1 v_{gs} + g_2 v^2_{gs} + g_3 v^3_{gs} + \ldots \tag{2.1}$$

where g_1 is the small-signal transconductance and the higher-order coefficients (g_2, g_3 etc.) define the strengths of the corresponding nonlinearities. Among these three

coefficients, g_3 is related to the third-order intermodulation distortion and the IIP3 of a FET is governed by g_3. Then,

$$A_{IP3} = \sqrt{\frac{4}{3}\left|\frac{g_1}{g_3}\right|}[V]. \tag{2.2}$$

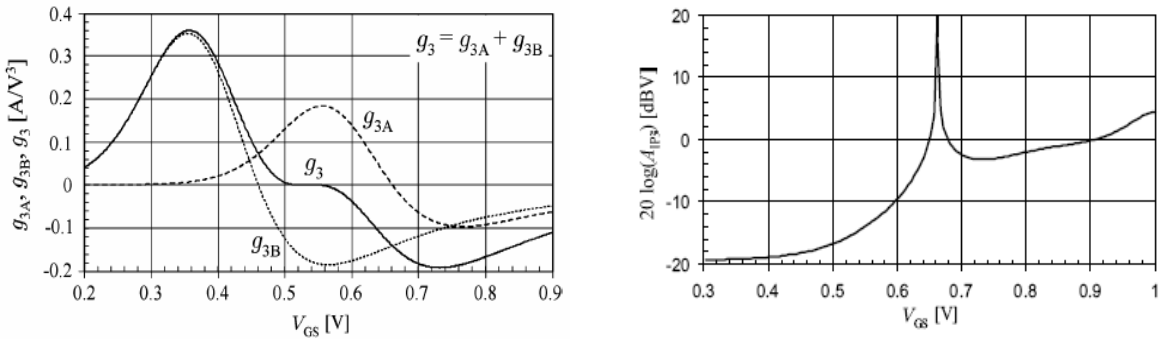
In general, the power series coefficients can be controlled by the dc gate-source and drain-source voltage, V_{GS} and V_{DS}. Also, the coefficients of (2.1) can be expressed by

$$g_1(V_{GS}) = \frac{\partial i_D}{\partial v_{GS}}, \tag{2.3a}$$

$$g_2(V_{GS}) = \frac{1}{2}\frac{\partial^2 i_D}{\partial v^2_{GS}} = \frac{1}{2}\frac{\partial g_1(V_{GS})}{\partial v_{GS}}, \tag{2.3b}$$

$$g_3(V_{GS}) = \frac{1}{6}\frac{\partial^3 i_D}{\partial v^3_{GS}} = \frac{1}{3}\frac{\partial g_2(V_{GS})}{\partial v_{GS}}. \tag{2.3c}$$

As shown in Figure 2.1(a) and (b), there is a V_{GS} at which g_3=0 and $A_{IP3} = \infty$. However, it is not easy task to find the optimum bias voltage because the peak has very narrow range.



(a) **(b)**

Figure 2.1 (a) Power series coefficients (b) Theoretical A_{IP3}

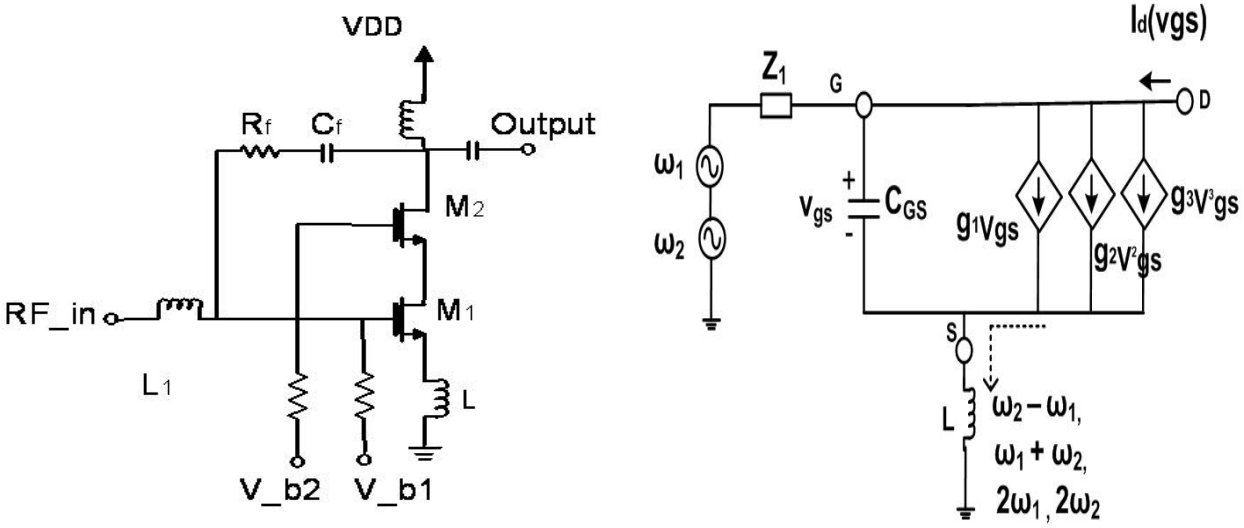
Figure 2.2(a) shows the schematic of the linearized LNA using optimum gate biasing technique and a small-signal nonlinear equivalent circuit of a FET is shown in Figure 2.2(b). L is the source degeneration inductance which creates a feedback path for the drain current to v_{gs}. The 2nd-order nonlinearity of i_d contributes to IM_3 because of this feedback. By the Volterra series analysis, the following expression for IIP3 can be derived [18]

$$IIP_3 = \frac{4g_1^{\,2}\omega^2 LC_{gs}}{3\left|\varepsilon(\Delta\omega, 2\omega)\right|} \tag{2.4}$$

where

$$\varepsilon(\Delta\omega, 2\omega) = g_3 - \frac{2g^{\,2}{}_2/(3g_1)}{1+\dfrac{1}{j2\omega L_{g_1}}+\dfrac{j2\omega}{\omega_T}+\dfrac{Z_1(2\omega)}{\omega_T L}}, \tag{2.5}$$

$\omega \approx \omega_1 \approx \omega_2$ *and* $\omega_T = g_1 / C_{GS}$. From (2.5), IIP3 shows the maximum value when g_3 is equal to the real part of the second term.



(a) **(b)**

Figure 2.2 (a) Schematic of a linearized LNA using optimum gate biasing (b) Small-signal nonlinear equivalent circuit of common-source FET

Advantages –

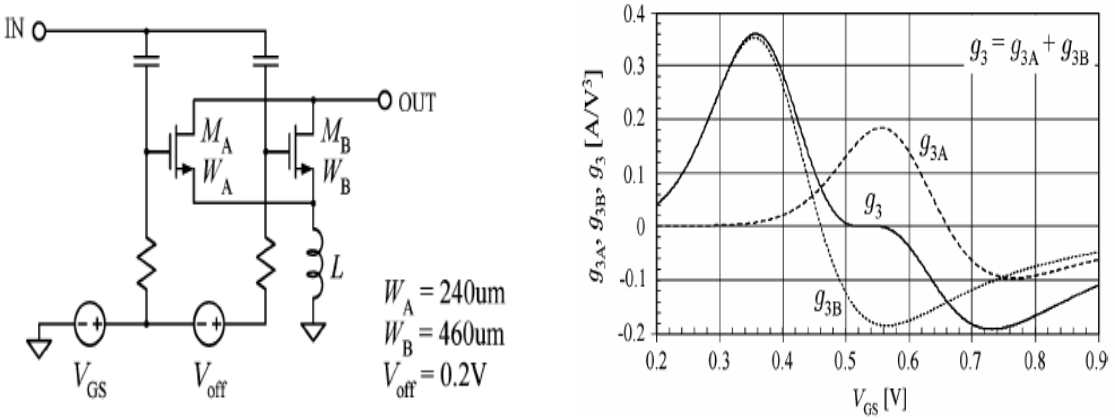
- A significant improvement in IIP3 at low frequencies.

Drawbacks –

- A manual tuning is required to achieve a significant improvement in IIP3
- Sensitive to process and temperature variations.

2.1.2. linearization using derivative superposition (DS) technique

One of efficient linearization methods for CMOS LNA is the derivative superposition (DS) technique which nulls the negative third-order derivative of the dc transfer characteristic (g_3) of the main FET by paralleling the auxiliary FET biased near the weak inversion region with the positive g_3. The DS method made it possible to reduce the IIP3 sensitivity to the bias voltage [8,9,10].



(a) **(b)**

Figure 2.3 (a) Schematic of a linearized LNA using DS method (b) Third-order power series coefficients

Figure 2.3(a) shows the circuit schematic of a LNA using DS method, and as can be seen from Figure 2.3(a) and Figure 2.3(b), the main FET M_A is in the weak inversion region near the peak in its positive g_3 with the optimum gate bias voltages. Also, the auxiliary FET M_B works in the strong inversion region [7].

By the Volterra series analysis, the following expression for IIP3 can be derived [7]

$$IIP_3 = \frac{4g_1{}^2\omega^2 LC_{gs}}{3|\varepsilon|} \tag{2.6}$$

$$\varepsilon = g_3 - \frac{2g_2{}^2/3}{g_1 + \frac{1}{j2\omega L} + j2\omega_0 C_{gs} + Z_s(2\omega)\frac{C_{gs}}{L}}. \tag{2.7}$$

Due to the second term in (2.7), an infinite IIP3 can not be acquired by just making g_3 zero and it means that this second term contributes the 2nd-order nonlinearity to IMD3.

Advantages –

- The IIP3 sensitivity to the gate bias voltage is decreased.
- Moderate IIP3 improvement is possible.

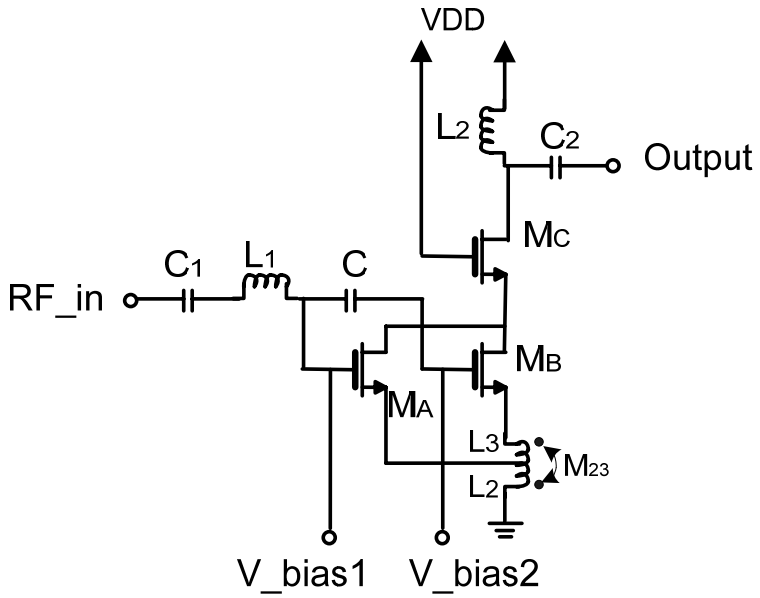
Drawbacks –

- The degradation of noise figure due to the additional noise from the auxiliary FET.
- Additional bias voltage is required.
- A small source degeneration inductance prevents a simultaneous noise-power input matching which produces a higher NF.

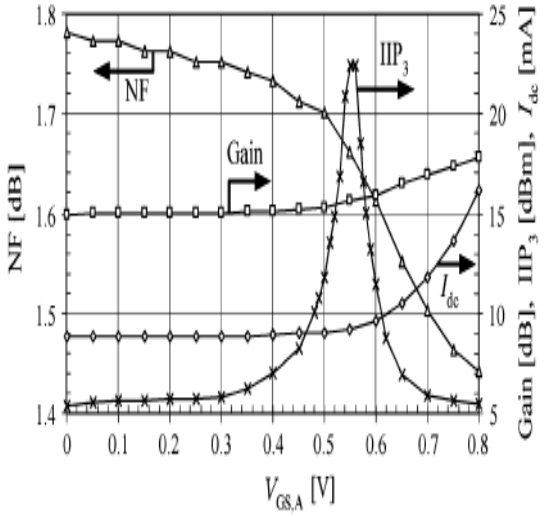
2.1.3. linearization using modified derivative superposition (MDS) technique

To overcome few drawbacks of the DS method, the modified DS method has been proposed [7]. The modified DS method uses two source-degeneration inductors in series with the conventional DS method. The CS FET sources are connected to different nodes of the inductor to adjust the magnitude and phase of the third-order nonlinearity contribution. It has been shown that the modified DS method outperforms the conventional DS method on IIP3 performance due to the contribution of the second-order nonlinearity to IMD3. The degradation of noise figure is a drawback for both the DS and modified DS method due to the additional noise from the auxiliary FET. Furthermore, the low power and low noise optimization techniques may not be easily applied due to the complicated noise model of the auxiliary FET. Then, as shown in Figure 2.4(a) and (b), the modified derivative superposition (MDS) method was proposed in [7] and it achieved +22-dBm IIP3 with 1.65-dB NF and 9.3 mA at 2.6 V power consumption.

As shown in Figure 2.4(a), the main FET M_A operates in weak inversion region with a positive g_{3A} and the auxiliary FET M_B operates in strong inversion region with a negative g_{3B}. To overcome the drawback of DS method, the source of the main FET is connected to the common node of two inductors, which changes the magnitude and phase of its g_{3A} contribution to IMD3.



(a)



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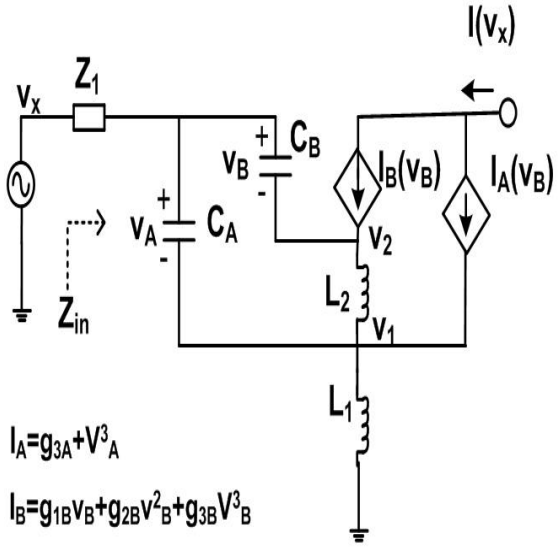


(c)

Figure 2.4 (a) Commonly used topologies of LNA with modified DS method (b) Measured IIP3 (c) Simplified equivalent circuit of the modified DS method

By the Volterra series analysis, the following expression for IIP3 can be derived [7]

$$IIP_3 \approx \frac{4g^2{}_{1B}\,\omega^2\left[L_1(C_A+C_B)+L_2C_B\right]}{3|\varepsilon|} \tag{2.8}$$

where
$$\varepsilon = g_{3A}(1+j\omega L_2 g_{1B})[1+(\omega L_2 g_{1B})^2] \times\left[1+\frac{L_2C_B}{L_1(C_A+C_B)+L_2C_B}\right] +g_{3B}-\frac{2g^2{}_{2B}}{3g_{1B}}\frac{1}{1+\frac{1}{j2\omega(L_1+L_2)g_{1B}}} \tag{2.9}$$

*Advantage*s –

- The highest IIP3 among known FET LNAs.

Drawbacks –

- The degradation of noise figure due to the additional noise from the auxiliary FET.
- Additional bias voltage is required and also two additional inductors are required.

2.2 Highly linear mixer

Mixers are widely used in modern communication systems to realize frequency translation of the carrier signals. The linearity of mixer in a receiver for multiband applications is one of key issues because the whole linearity of a receiver is often limited by the first down-conversion mixer due to a relatively large signal level compared with the input signal level of LNA. Intermodulation distortion in the mixer greatly affects the dynamic range of most communication systems. Therefore, the mixer determines the achievable second-order input intercept point (IIP2) and third-order input intercept point (IIP3) of the receiver. In CMOS downconversion mixers, there are several mechanisms which generate second-order intermodulation distortion [8]: self-mixing, transconductor nonlinearity, switching pairs nonlinearity, and mismatch in load resistors. Due to coupling into the local oscillator port, the RF signals self-mix. Self-mixing can be significantly reduced by means of layout techniques which decrease coupling effects between the RF and LO signals. Active devices inherently generate second-order intermodulation distortion components because they have nonlinearities in the *I-V* characteristic. A perfectly matched switching stage up-converts the input differential baseband spectrum at mixer output.

The IIP3 of transconductance stage can be analyzed with classical technique [9, 10]. However, little has been published on the IIP3 characteristics of the CMOS switching pair. The most analytical method for the CMOS switching pair was done by using time-varying power series in low frequencies and time-varying Volterra series in high frequencies [11].

Some commercially available receivers employ an RF inter-stage surface acoustic wave (SAW) filter to suppress the signal leaking from the transmitter. This inter-stage SAW filter relaxes the linearity requirements on the mixer. However, this method requires an off-chip component and an additional LNA.

2.2.1 RF nonlinearity of active CMOS mixers

Linearity analysis of single-balanced CMOS mixer

Figure 2.5(a) and (b) shows a single-balanced CMOS mixer and its nonlinear model of transconductance stage to derive the nonlinear equations. In Figure 2.5(b), V_s is the voltage signal source, Z_g is the impedance at the gate of RF transconductance stage, which includes source resistance R_s , gate resistance R_g. Three main sources of nonlinearity are $g_m V_{gs}$, C_{gs} and C_{gd} . The feedback (Miller) capacitor effect is significant in determining the input impedance of RF circuit and will effect IIP3 of RF circuit.

By applying Kirchhoff's voltage law in Figure 2.5(b),

$$V_s = (Z_g + R_g)(I_{gs} + I_{gd}) + V_{gs} + Z_s(I_{gs} + g_m V_{gs} + I_{ds}) \tag{2.10}$$

where

$$I_{ds} = \frac{g_{ds}(sC_{ds}V_{gs} + I_d - g_m V_{gs})}{g_{ds} + sC_{gs}}$$

$$I_{gd} = g_m V_{gs} - I_d + \frac{g_{ds}(sC_{gd}V_{gs} + I_d - g_m V_{gs})}{g_{ds} + sC_{gs}}.$$

The Volterra series expression for I_d is derived as

$$I_d = A_1(s)V_s + A_2(s_1, s_2)V_s^2 + A_3(s_1, s_2, s_3)V_s^3 + ... \tag{2.11}$$

where $A_1(s)$, $A_2(s_1, s_2)$ and $A_3(s_1, s_2, s_3)$ are the first three Volterra seires coefficients, given by

$$A_1(s) = T_1 C_1(s)$$

$$A_2(s_1, s_2) = T_1 C_2(s_1, s_2) + T_2 C_1(s_1) C_1(s_2) \tag{2.12}$$

$$A_3(s_1, s_2, s_3) = T_1 C_3(s_1, s_2, s_3) + 2T_2 \overline{C_1 C_2} + T_3 C_1(s_1) C_1(s_2) C_1(s_3).$$

T_1, T_2 and T_3 are the first three Taylor series coefficients of the drain current, and $C_1(s)$, $C_2(s)$ and $C_3(s)$ are the first three Volterra series coefficients of the gate-source voltage. Therefore,

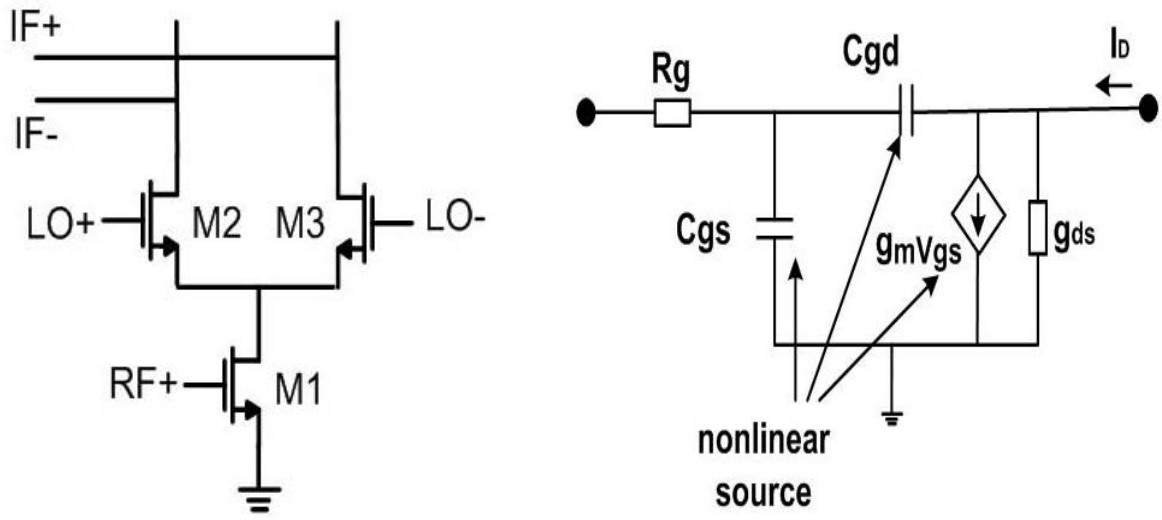
$$\left|IM_3(\omega_1, \delta\omega, L_s)\right| = \left|\frac{3A_1^3(\omega_1)}{T_1^4}\right| \left|1 + j\omega C_{gs}\left[Z_s(\omega_1, L_s) + Z_g(\omega_1, L_s)\right]\right|$$

$$\times \left|T_3 - 2T_2 \rho(\omega_1, \delta\omega, L_s)\right| M^2 \tag{2.13}$$

where $\rho(\omega_1, \delta\omega, L_s) = T_2 / T_1 \left[2A_1(\delta\omega, L_s) Z_s(\delta\omega, L_s) + A_1(2\omega_1, L_s) Z_s(2\omega_1, L_s)\right]$ and $\delta\omega = \omega_1 - \omega_2$. Here, the magnitude of IM_3 depends on

$$\left|1 + j\omega C_{gs}\left[Z_s(\omega_1, L_s) + Z_g(\omega_1, L_s)\right]\right|$$

where the inductive degeneration , $j\omega C_{gs} Z_s(\omega_1, L_s)$, is a negative real number.



(a) **(b)**

Figure 2.5 (a) Single-balanced CMOS mixer (b) Nonlinear model of single-balanced mixer transconductance stage

Linearity analysis of double-balanced CMOS mixer

Figure 2.6(a) and (b) shows a single-balanced CMOS mixer and its nonlinear model of transconductance stage to derive the nonlinear equations. Ideally, the output of the double-balanced mixer's transconductance stage is linearly proportional to the input level and the linearity of a double-balanced mixer is better than that of a single-balanced mixer without any degeneration. However, in reality, because of sub-square law behavior and negative feedback, the linearity of a double-balanced mixer is even worse. By applying Kirchhoff's voltage law in Figure 2.6(b),

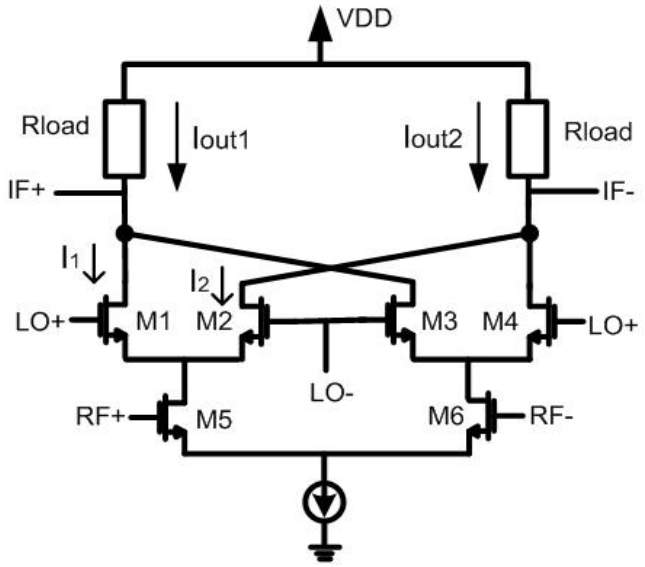
$$V_s = X_1(V_{gs1} - V_{gs2}) + X_2(I_{d1} - I_{d2}) \tag{2.14}$$

$$0 = Y_1(V_{gs1} + V_{gs2}) + Y_2(I_{d1} + I_{d2}) \tag{2.15}$$

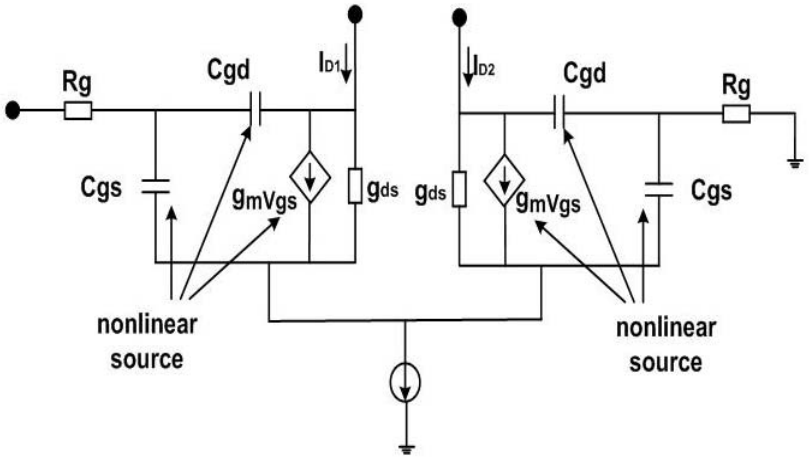
where

$$Y_1 = jwC_{gs} + g_m + \frac{g_{ds}(jwC_{gd} + g_m)}{g_{ds} + jwC_{gs}}, \quad Y_2 = \frac{g_{ds}}{g_{ds} + jwC_{ys}}.$$

$$X_1 = 1 + (Z_g + Z_s + R_g)Y_1, \quad X_2 = (Z_g + Z_s + R_g)Y_2 - (Z_g + R_g)$$



(a)



(b)

Figure 2.6 (a) Double-balanced CMOS mixer (b) Nonlinear model of double-balanced mixer transconductance stage

Solving (2.14) and (2.15) gives the following Volterra series expressions

$$I_{d1} = B_1(s)V_s + B_2(s_1, s_2)V_s^2 + B_3(s_1, s_2, s_3)V_s^3 + ... \quad (2.16)$$

$$I_{d2} = -B_1(s)V_s + B_2(s_1, s_2)V_s^2 - B_3(s_1, s_2, s_3)V_s^3 + ... \quad (2.17)$$

where $B_1(s)$, $B_2(s_1, s_2)$ and $B_3(s_1, s_2, s_3)$ are the first three Volterra series coefficients.

$$B_1(s) = T_1 D_1(s)$$

$$B_2(s_1, s_2) = T_1 D_2(s_1, s_2) + T_2 D_1(s_1) D_1(s_2)$$

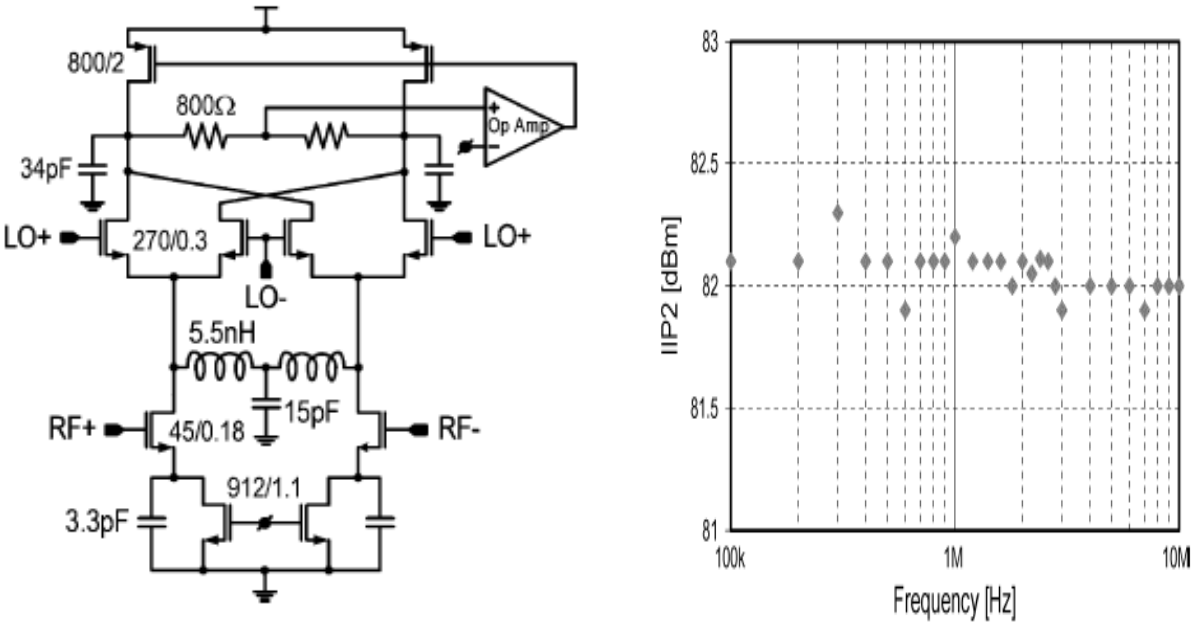
$$B_3(s_1, s_2, s_3) = T_1 D_3(s_1, s_2, s_3) + 2T_2 \overline{D_1 D_2} + T_3 D_1(s_1) D_1(s_2) D_1(s_3).$$

2.2.2. A highly linear mixer with RC degenerated technique

An efficient method was proposed to improve IIP2 and IIP3 performance as shown in Figure 2.7(a). In this method, the input transconductor is RC degenerated, the output resistors are matched, and the parasitic capacitance at the node between the switching pairs and the input stage is tuned out [20]. To implement a high IIP2, a fully differential RF transconductance stage is suitable due to the low common-mode gain at low frequencies and a pseudodifferential RF stage is a good candidate for a high IIP3 mixer.

As can be seen from Figure 2.7(a), the FET connected parallelly with the capacitor (3.3 pF) degenerate the RF input devices providing low gain at low frequency for higher IIP2. This capacitor (3.3 PF) can reduce third-order inter-modulation distortion leading to high IIP3 because it is grounded at RF frequency. The main idea is filtering out

the fundamental LO frequency, together with side-bands, with a significant improvement in IIP2 performance. Also, inductor (5.5 nH) is chosen to resonate out the parasitic capacitance, Cp, at the local oscillator frequency. This work has achieved +78 dBm IIP2 and +10 dBm IIP3 with 7.2 mW power consumption.



(a) **(b)**

Figure 2.7 (a) High linear mixer with LC filter (b) Measured IIP2

*Advantage*s –

- Very high IIP2 and IIP3 performance.
- Any off-chip filter is not required because the LC filter suppress the 2nd harmonic.

Drawbacks –

- Additional two inductors and three capacitors are required.
- The total size of the mixer is bigger than the conventional Gilbert-type mixer.

CHAPTER III

Low Flicker-Noise Receiver Front-end

3.1 Flicker noise

Low frequency noise in silicon MOSFET's is dominated by flicker noise. It is commonly known as 1/f noise since the noise spectral density is inversely proportional to frequency. Because MOSFET's have large flicker noise, it sets a lower limit to the level of signal that can be processed by circuits. In a CMOS receiver, the mixer is the main source of flicker noise generation.

3.1.1. Device model

As shown in Figure 3.1, since the silicon crystal reaches an end at the interface between the gate oxide and the silicon substrate, many "dangling" bonds appear, giving rise to extra energy states. As charge carriers move at the interface, some are randomly trapped and later released by such energy states, introducing flicker noise in the drain current [54]. Among the different types of noise mechanisms present in semiconductors, low-frequency noise, also known as 1/f noise due to its typical 1/f dependence on frequency, is, perhaps, the least understood. There exists no one theory that can explain the origin of this type of noise across different types of semiconductor structures. Hence,

it becomes necessary to evaluate this noise for each technology generation to understand the impact of scaling.

There are two different theories that can explain the physical origins of flicker noise. In the carrier density fluctuation model, originally proposed by McWorther [12], the noise is explained by the fluctuation of channel free carriers due to the random capture and emission by the Si-SiO2 interface traps known as slow rates.

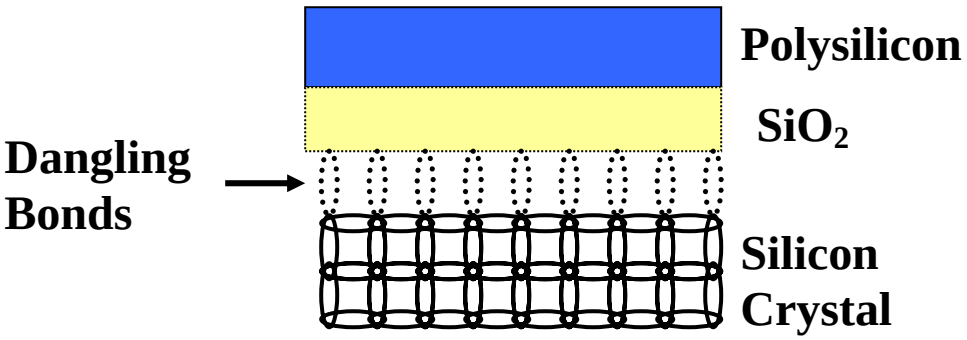


Figure 3.1 Dangling bonds at the oxide-silicon interface

Using this model, the input referred noise is independent of the gate bias voltage and the magnitude of the noise spectra is proportional to the density of the interface trap. On the other hand, the mobility fluctuation model, first proposed by Hooge [13], suggests the gate voltage dependence in the input referred noise. The model is based on the empirical experimental observation of the noise in the homogeneous samples, and the input referred noise shows strong gate bias dependence. In the n-channel transistors, the input referred noise shows no gate bias dependence when the gate bias is varied from subthreshold to strong inversion. This suggests that flicker noise in n-channel devices

follows carrier density fluctuation. In the p-channel devices, strong gate-bias dependence in the input referred noise is observed. Mobility fluctuation seems to be able to explain the p-channel noise behavior. The unified model with a functional form resembling the number fluctuation model at low bias and the mobility fluctuation model at high bias has been proposed and this unified noise model is often used as the basis for circuit simulations, like BSIM3. This model describes the flicker noise of n- and p-type MOSFETs in all operating regimes. The BSIM3v3 model is based on the unified theory. Only expression valid in the inversion region are shown as an illustration. Details on the BSIM3v3 model can be found in [14].

$$S_{ID} = \frac{kTq^2 |I_D| \mu_{eff}}{\alpha_t f^{EF} L_{eff}{}^2 C_{OX}} \left[\begin{array}{l} NOIA \ln \frac{N_O + N^*}{N_L + N^*} + NOIB(N_O - N_L) + \\ \frac{NOIC}{2}(N_O{}^2 - N_L{}^2) \end{array} \right]$$

$$+\Delta L_{clm} \frac{kTI_d{}^2}{\alpha_t f^{EF} W_{eff} L_{eff}{}^2} \frac{NOIA + NOIBN_L + NOICN_L{}^2}{\left(N_L + N^*\right)^2} \tag{3.1}$$

$$with$$
$$qN_O = C_{OX}\left(|Vgs - Vth|\right)$$
$$qN_L = C_{OX}\left(|Vgs - Vth - Vds|\right)$$
$$N^* = \frac{kT(C_{OX} + C_d + C_{it})}{q^2}$$

The simplified level-3 HSPICE model is

$$S_{id} = \frac{K_f gm^2}{C_{ox} W_{eff} L_{eff} f^{AF}} \tag{3.2}$$

where K*f* is a process parameter, W*eff and* L*eff* are the effective width and length, C*ox* is the oxide capacitance. This model is not as accurate as the BSIM3v3 model, but serves as a guiding empirical formulation and has been used extensively to model flicker noise for first-order approximate solutions.

Test results indicate similar flicker noise performance of NMOS and PMOS devices at all tested inversion levels for devices with L >= 2 um. For smaller L, the PMOS devices exhibit much improved noise performance over their NMOS counterparts, especially in weak inversion. As the process technology scales down, the corner frequencies of the low frequency noise, also known as flicker noise or 1/f noise, tend to become higher. It is also demonstrated that the dual gate oxide process, which provides both thin and thick gate oxide transistors in a single process technology, produces thin gate oxide transistors with better flicker noise performance than their counterparts from the single gate oxide process. This is most likely due to the lowering of the nitrogen concentration peak at the Si/SiO2 interfaces causing 1/f noise improvement.

Figure 3.2 shows the measured noise spectral density of n-channel devices with L=0.18 um, W=60 um, and W=120 um. This measurement was done by using Agilent 35670A Dynamic Signal Analyzer. As seen from Figure 3.2, the intrinsic flicker noise is inversely proportional to the WL of the device. The device sizes shown in Figure 3.2 were used for designing mixers in Chapter V.

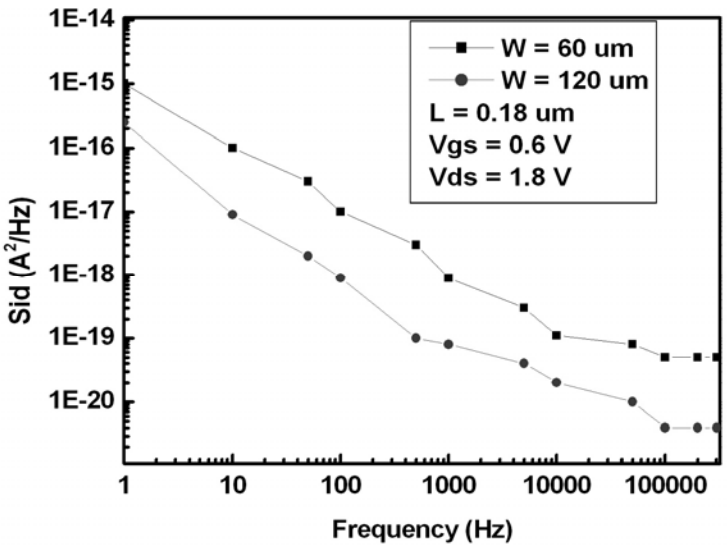


Figure 3.2 Measured current noise spectrum for NMOS devices with L=0.18 um, W=60 um, and W=120 um

3.1.2. Switching mixer fundamentals

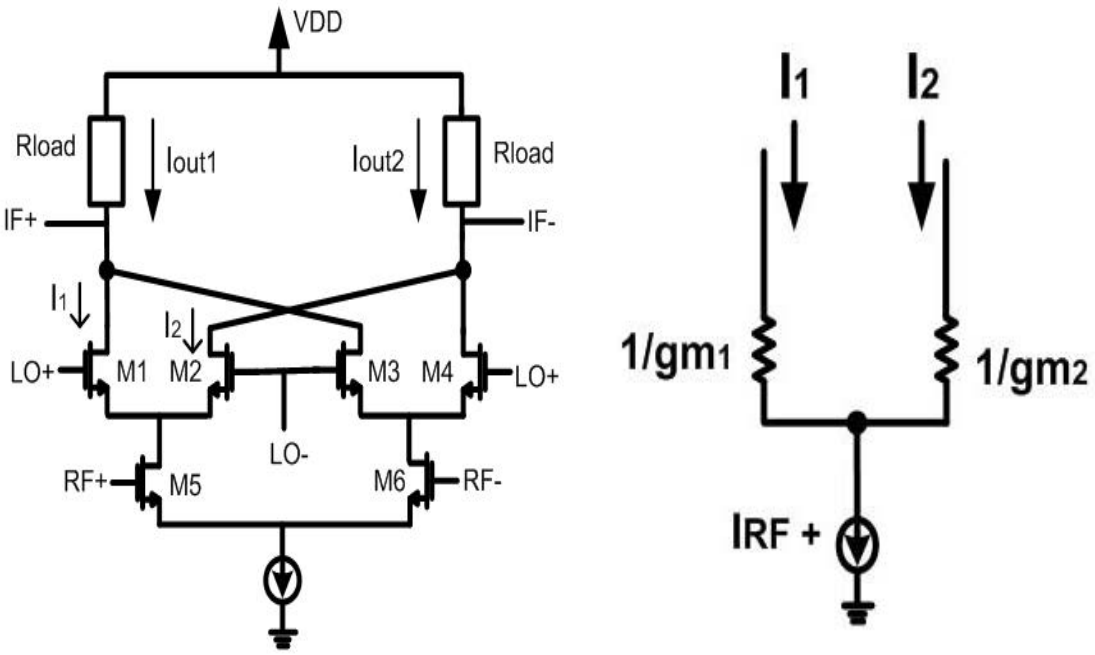
Mixers are widely used in modern communication systems to realize frequency translation of the carrier signals and also are the main source of flicker noise generation in CMOS receiver front-ends. Active mixers which employ a switching transistor pair for current commutation, such as the Gilbert cell, are frequently used, because they have advantages such as high conversion gain and high port-to-port isolation. Figure 3.3(a) shows a conventional double-balanced Gilbert-type mixer. The mixer comprises an RF input transconductance stage, LO switches, and output loads. The transconductance stage is used to transform the input voltage signal to current, which is then commutated with LO switching switches. The output current is

$$I_o = I_{out1} - I_{out2} = (I_1 - I_2) - (I_4 - I_3). \tag{3.3}$$

From (19), the difference of the output currents of two single-balanced mixers becomes the output of the Gilbert cell. Therefore, the output current of the single-balanced mixer of Figure 3.3(b) is a function of $V_{LO}(t)$, I_{RF} and i_{RF} [15]

$$I_{out1} = I_1 - I_2 = F(V_{LO}(t), I_{RF} + i_{RF}) \tag{3.4}$$

where $V_{LO}(t)$ is the instantaneous LO voltage, I_{RF} is the bias current for the RF trasnconductor and i_{RF} is the small-signal current for the RF transconductor. By using a first-order Taylor expansion [15]



(a) **(b)**

Figure 3.3 (a) Double-balanced Gilbert-type mixer (b) Equivalent model of the single-balanced mixer

$$I_{out1} = I_1 - I_2 = F(V_{LO}(t), I_{RF}) + \frac{\partial}{\partial I_{RF}} F(V_{LO}(t), I_{RF}) \cdot i_{RF} \tag{3.5}$$

or

$$I_{out1} = I_1 - I_2 = p_o(t) + p_1(t) \cdot i_{RF} \tag{3.6}$$

where $p_o(t)$, $p_1(t)$ are periodic waveforms and i_{RF} is the small-signal current at the output of the RF transconductor. As shown in Figure 3.3(b), by current division,

$$p_1(t) = \frac{g_{m1}(t) - g_{m2}(t)}{g_{m1}(t) + g_{m2}(t)} \tag{3.7}$$

where $g_{m1}(t)$ and $g_{m2}(t)$ are the transconductances of switching stages [15]. $p_o(t)$ is eliminated in a double-balanced mixer with perfect device matching. Also, a first-order approximation of the conversion gain, Gc, of the mixer becomes [15]

$$Gc \cong \frac{2}{\pi}\left(\frac{\sin(\pi f_{LO} t_{sw})}{\pi f_{LO} t_{sw}}\right) \cdot gm_{RF} \tag{3.8}$$

where f_{LO} is the LO frequency and t_{sw} is the ON-and-OFF switching times for the LO signal.

3.1.3. Flicker noise mechanism

Direct conversion architectures offer the unique advantage of a relaxed image rejection. Nonetheless, direct conversion architectures suffer from some peculiar drawbacks, the most important being DC offset, local oscillator (LO) leakage, and 1/f noise. This is very important since the mixer is the key block of a direct conversion receiver whose 1/f noise tends to limit the receiver signal to noise ratio. Passive CMOS mixers are usually considered the best choice for direct conversion receivers, since they do not contribute 1/f noise, at least in principle, provided no DC current is flowing in the MOS devices. Due to the mixer loss, a very high LNA gain is required to minimize the baseband noise contribution. This high gain at RF is hard to handle and can easily produce oscillations.

1/f noise performances of the mixer are primarily determined by the switching pair devices. On the other hand the transconductance times IIP3 product is primarily determined by the input stage. In a traditional Gilbert cell as shown in Figure 3.3(a), the two stages are fed by the same current. For the 1/f noise optimized mixer design, the input stage and the switching stage currents can be set independently to simultaneously optimize noise figure, linearity, and gain. A pMOS mixer can be used because this is the one that gives the best 1/f noise performances. We can separately consider the 1/f noise contribution depending on the output stage, input stage, and switching pair stage. The output stage is realized by means of resistors, connected between the output nodes and ground, and they do not produce significant 1/f noise. The input stage devices do not produce, to first order, any 1/f noise at the output, in the frequency band of the signal. In

fact, their 1/f noise is up-converted and does not appear at baseband. On the other hand, the 1/f noise of the switching devices directly contributes to the mixer noise. The first mechanism that was recognized to contribute 1/f noise is the direct one, due to finite slope of the switching pair transitions.

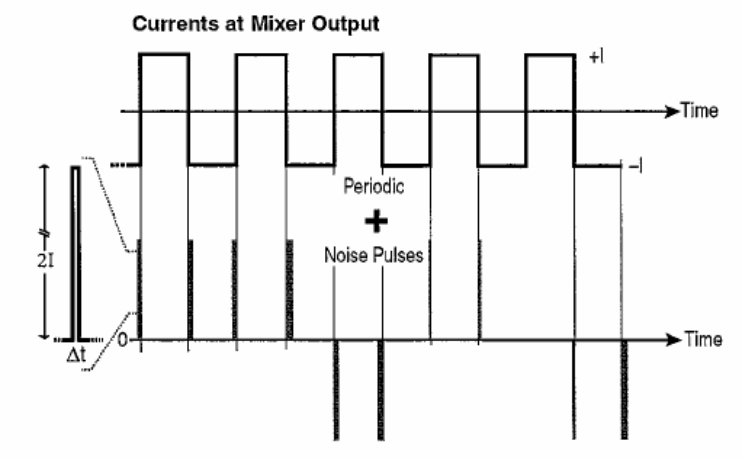


Figure 3.4 Mixer output current with noise pulse

The LO switches generate noise pulse trains as shown in Fig. 3.4 by the direct mechanism and the DC average of noise pulse trains is the output flicker noise current as shown below [5]

$$i_{o,n(dir)} = \frac{2}{T} \times 2I \times \Delta t = \frac{2}{T} \times 2I \times \frac{Vn}{S} = \frac{(4I \times Vn)}{(S \times T)} \tag{3.9}$$

$$Vn = \sqrt{2 \times \frac{K_f}{W_{eff} L_{eff} C_{ox} f}} \tag{3.10}$$

where I is the bias current for the RF transconductance stage, T is the LO period, V_n is the equivalent flicker noise of the switching pair, and S is the slope of the LO signal. Also, W_{eff} *and* L_{eff} are the effective width and length, C_{ox} is the oxide capacitance, f is

frequency, and K_f is a process parameter [5]. From (3.9), it is worth noticing that low-frequency noise at the gate of switch, Vn, appears at the output directly and the output flicker noise current is decreased if the product of the slope of the LO signal at zero-crossing and its period [5]. According to (3.10), Vn is inversely proportional to the WL of the device. By using (3.9) and (3.10), the SNR at the mixer can be derived

$$SNR = \frac{S \cdot T}{2\pi (V_{GS} - V_t)} \cdot \frac{V_{in}}{V_n}. \tag{3.11}$$

From (3.11) and Figure 3.5, it is shown that SNR improves by raising the product of the slope of LO waveform at zero-crossing and its period.

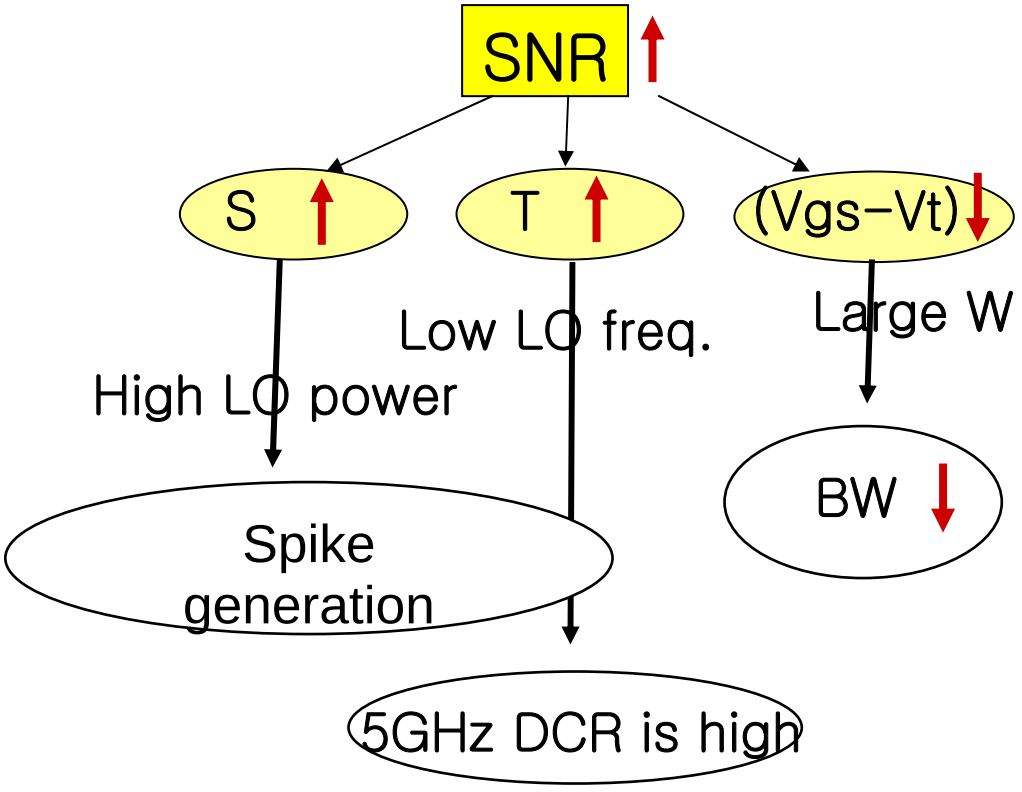


Figure 3.5 SNR at the mixer output by direct mechanism

Also, it can be improved by increasing the gate area of the LO switch to lower V_n or by lowering the overdrive voltage, $V_{GS} - V_t$, of the transconductance RF stage. However, mixer bandwidth will be degraded by increasing the gate area for LO switch or lowering the overdrive voltage. In order to decrease flicker noise in the direct mechanism, a popular method is to reduce the width of the noise pulses, which can be implemented by reducing the value of V_n. To reduce the value of V_n, the size of the switching pairs needs to be increased, and large switching devices increase the parasitic capacitance of the switching pairs. Minimizing the flicker noise due to the direct mechanism leads to large area switching devices (in order to minimize the equivalent flicker noise voltage) and low biasing currents, i.e., low overdrive voltages (in order to minimize the switching time). Both these design choices lead to low f_T for the switching devices. For large switching stage currents, the conversion gain is constant and the input and output noise reduce with a biasing current reduction. For lower current values, when $\omega_{LO} \approx g_m/C$, with g_m the switching devices transconductance and C the capacitive parasitic loading the common source, the conversion gain starts to decrease due to ac loss.

This second noise mechanism, the indirect one, where it is shown that the equivalent noise voltage in series with the gate periodically charges and discharges the tail capacitance producing an average output noise current. As a result, to minimize its contribution to the input referred noise power spectral density, the switching stage has to be biased in the bandwidth limited region ($\omega_{LO} > g_m/C$), i.e., low biasing current and large area devices. Once this operation region is chosen, the optimum biasing current will be determined by the required mixer conversion gain.

The optimum biasing current of the switching and input stages are different. A

relatively low current is used to bias the switching stage whereas the input stage biasing current determines the mixer gain and IIP3. The higher the input stage biasing current, the higher its IIP3 times transconductance product. The switching stage can employ p-channel devices. This is valuable when, the lower 1/f noise coefficient of p-channel devices overcompensates the lower transition frequency. As a result, the 1/f noise contribution is lower using a pMOS switching stage rather than an nMOS one.

The optimum device dimensions are derived as follows: 1) increasing the device width produces a reduction of the noise figure up to a maximum value, beyond which the noise figure remains almost constant. In fact, increasing the gate width produces a reduction in the 1/f noise coefficient (K_f), but also an increase in the capacitance loading the common source. When the loss of gain compensates the reduction in 1/f noise coefficient, no improvement is found and 2) non-minimum channel lengths are selected to lower the noise figure. In fact K_f is inversely proportional to the device length. Actually, an optimum device length exists, since the noise gain increases with a length increase. Moreover, the tail capacitance increases with the device length, reducing the conversion gain. As highlighted above, the switching pair stage is the main responsible of 1/f noise. All the other noise sources do not contribute noise at baseband, at least in principle. Nonetheless, nonidealities such as, for example, switching pair mismatches can lead to 1/f noise contribution coming from the input stage. The threshold voltage mismatch is inversely proportional to the device area. The current and the aspect ratios of the RF input transconductor devices are fixed by noise and linearity constraints. Therefore their transconductances cannot be changed. Notice that the RF devices 1/f noise contribution does not depend on the switching stage biasing current and it is

typically much smaller than the contribution of the switching pairs themselves. However, if the switching stage biasing current is much smaller than the RF input stage one, the noise contribution of the latter might become important. In this case, nonminimum channel lengths might be chosen with the drawback of an increased mixer RF input capacitance. For an extremely low flicker noise design attention must be paid even to the biasing circuits. In particular, the current mirrors setting the current of the RF input transconductors should be realized with long channel devices.

The flicker noise at the RF transconductance stage will be upconverted and has no contribution at the baseband. Only switching transistors contribute flicker noise at the output. Therefore, the ratio of the flicker noise gain to the RF signal gain is the measure of the noise performance. The smaller the ratio is, the better is the noise performance. The flicker noise gain is measured from the LO input to the mixer output. Firstly, the effect of the output bandwidth and switching frequency is studied. The transistors switch from the off state to the saturation region. The width of the switch transistor is used to change the output bandwidth and its effect on the input referred flicker noise is not considered. When the switching frequency is much less than the output bandwidth, the output flicker noise is bandwidth-independent. As the switching frequency is increased, the output flicker noise gets larger and the signal gain becomes smaller. Subsequently, the input referred noise gets much larger. For better noise performance, higher output bandwidth or lower switching frequency is preferred. The LO swing is another important factor for consideration. The larger the LO swing is, the better is the noise performance. In this case, the on-state gate voltage almost keeps constant due to the fixed biasing current. The off-sate gate voltage of the switch decreases with the swing. As we

mentioned before, to reduce flicker noise, a lower off-state gate voltage is needed. In other words, the large LO swing improves the noise performance. The effect of the bias current of mixer is also studied. Both the flicker noise gain and RF signal gain increase with the bias current. However, the flicker noise gain increases more quickly. That means the smaller the current is, the better the flicker noise performance is. It is opposite to the thermal noise. Therefore, the bias current should be as small as possible as long as the thermal noise performance is satisfied. Finally, we studied the effect of the transistor size of the switch. The larger the width, the better is the noise performance. However, when the transistor width is too large, the output bandwidth effect will appear and the noise performance will become worse. Also, the oscillator cannot afford a very large capacitive loading. That is to say the upper limit is bounded by LO driving ability and the output bandwidth. Experimental results show that there is a minimum point for input-referred flicker noise. When the transistor size is increased, it is found that the optimal bias point moves towards the weak inversion region. To reduce the flicker noise, the RF part can be biased near this region. At a biasing current, a larger W/L ratio drives the device toward the moderate or weak inversion region. This is very different from conventional mixers and offers the following advantages: the gain will be increased because transconductance increases with the W/L ratio and the maximum value will be achieved in this region; the thermal noise will be decreased; the l/f noise will also decrease because of the large transistor size and it is near the optimal region; the inductive load of the LNA can be smaller; and f_T of the device will not degrade too much. In the indirect mechanism, flicker noise mainly depends on the tail capacitance [5]. The average of the output noise current generated by the indirect mechanism is [5]

$$i_{o,n(ind)} = \frac{2}{T}\int_0^{\frac{T}{2}} i_{Cp}(t)dt = \frac{2}{T}\int_0^{\frac{T}{2}} C_p\left[\frac{d}{dt}V_s(t)\right]dt. \tag{3.12}$$

$$i_{o,n(ind)} = \frac{2}{T}C_p\left(V_s\left(\frac{T}{2}\right) - V_s(0)\right) = \frac{2}{T}C_pV_n. \tag{3.13}$$

where C_p is the tail capacitance of the node between the LO switches and the RF transconductance stage, T is the LO period, $V_s(t)$ is the voltage at the tail of the switching pair, and V_n is the equivalent flicker noise of the switching pair. According to (3.13), the tail capacitance should be small enough to decrease the effect of the indirect mechanism. Also, the SNR for indirect mechanism is shown in Figure 3.6, and it is given by

$$SNR = \frac{g_m\frac{2}{\pi}}{2f_{LO}C_p}\cdot\frac{V_{in}}{V_n} = 2\frac{f_T}{f_{LO}}\cdot\frac{V_{in}}{V_n}. \tag{3.14}$$

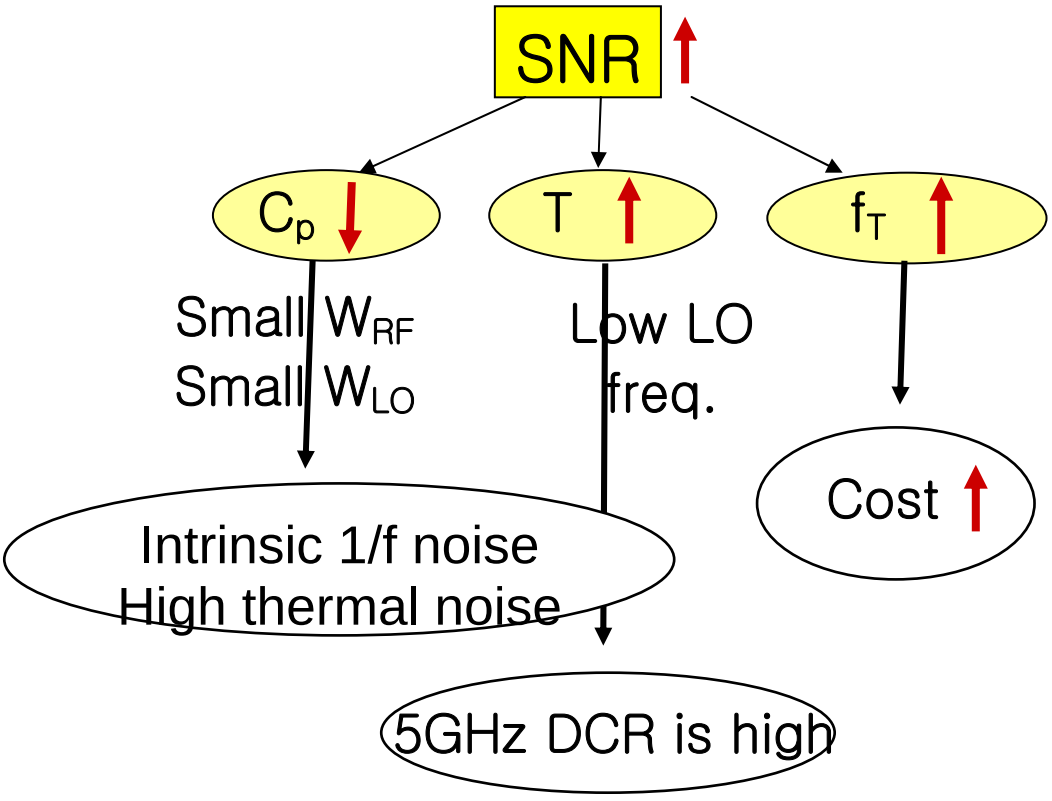


Figure 3.6 SNR at the mixer output by indirect mechanism

3.2 Low flicker-noise mixer

3.2.1 Static current bleeding technique

In a single balanced or a double balanced CMOS Gilbert cell mixer, higher gain and better linearity can be achieved by the bias current for the RF transconductance stage, but it also increases the bias current for the LO switching stages. Therefore, it causes voltage headroom issues when resistive loads are used at the output. Also, if the bias current for LO switching stages is increased, the larger driving voltage for LO stages is required. Then, voltage-controlled oscillator (VCO) has to generate more power for larger LO signal and it will increase the total receiver power.

The static current bleeding technique has been proposed to increase the bias current for the RF transconductance stage without increasing the bias current for the LO switching stages as shown in Figure 3.7. By using the static current bleeding technique, voltage headroom problem can be resolved and smaller LO driving voltage is required.

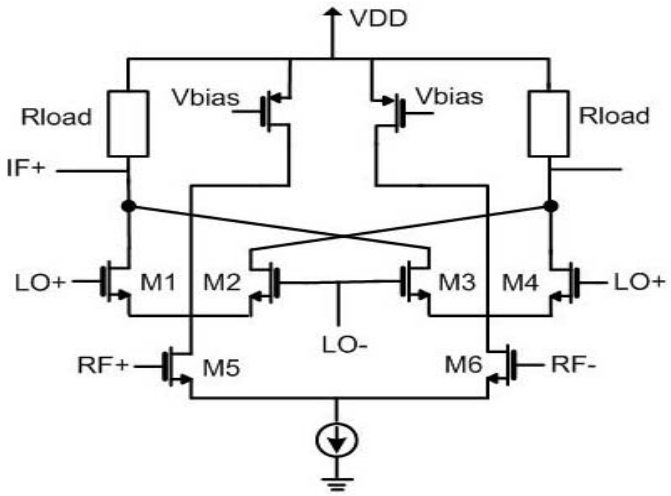


Figure 3.7 Low flicker-noise mixer with static current injection

Advantages –

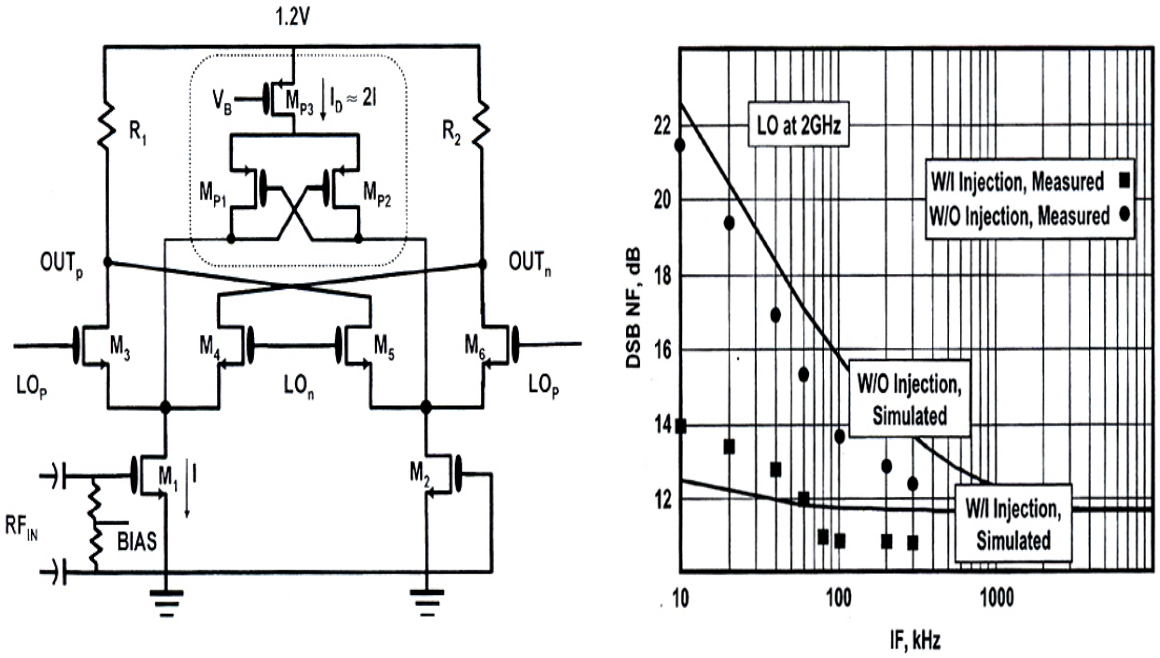
- Moderate simple technique to implement.
- The mixer bandwidth and its linearity are not degraded.
- Good conversion gain can be acquired.
- Small driving voltage for LO switching stages is required → Low power receiver.

Drawbacks –

- Reducing the bias current of the switches raises the impedances seen at their sources, allowing more RF current to be shunted by the parasitic capacitances at those nodes.
- The high impedances seen at their sources would reduce the mixer bandwidth and degrade its linearity.
- The white noise of the current source adds to that of the transconductance stage, increasing the mixer white noise figure.

3.2.2. Dynamic current injection technique

Flicker noise of the mixer can be reduced by decreasing the height of noise pulses. To decrease the height of noise pulses, the bias current of the mixer switches should be reduced and also the noise pulses are only generated at the switching instant of the LO differential pairs. Therefore, as shown in Figure 3.8(a), the dynamic current injection technique which injects a current at only the switching event has been proposed [21].



(a) **(b)**

Figure 3.8 (a) Low flicker-noise mixer with dynamic current injection (b) Mixer DSB noise figure with and without improvement

As shown in Figure 3.8(a), it injects a dynamic current equal to the bias current of each pair at only the switching event through a control circuit. The switching event is estimated through monitoring the voltage at the common-source node of each pair. Figure 3.8 (b) shows the simulated and measured double-sideband (DSB) noise figure over the

output frequency range of 10 kHz and 10 MHz. The noise figure of the same mixer without injection circuitry is measured as well for the comparison purposes. Both mixers shows similar white noise figure of about 11 dB. However, the flicker corner frequency of the mixer with dynamic injection is 10 kHz, whereas that of the original mixer without dynamic injection is 90 kHz.

Advantages –

- Sufficient to eliminate the output flicker noise.
- This technique does not add its own white noise since it is only ON at the switching event .
- The mixer bandwidth and its linearity are not degraded.
- The input impedance seen at the LO switches remain the same over the switching period.

Drawbacks –

- Larger LO power than a normal switching operation is required to turn the control circuit ON and OFF.
- The conversion gain is very low as an active mixer.
- If the switches mismatch, an accurate synchronization with LO signal may not be possible.

3.2.3. Passive mixer technique

Passive CMOS mixers are usually considered the best choice for direct conversion receivers, since they do not contribute 1/f noise, at least in principle, provided no DC current is flowing into the MOS devices. However, due to the mixer loss, a very high gain is required to minimize the baseband noise contribution. A high gain in RF is hard to handle and can easily produce oscillations. The work in [22] showed a 70 kHz low flicker-noise corner frequency with high linearity by using a low-impedance loaded double-balanced passive mixer. However, DC offset cancellation was not given in [22].

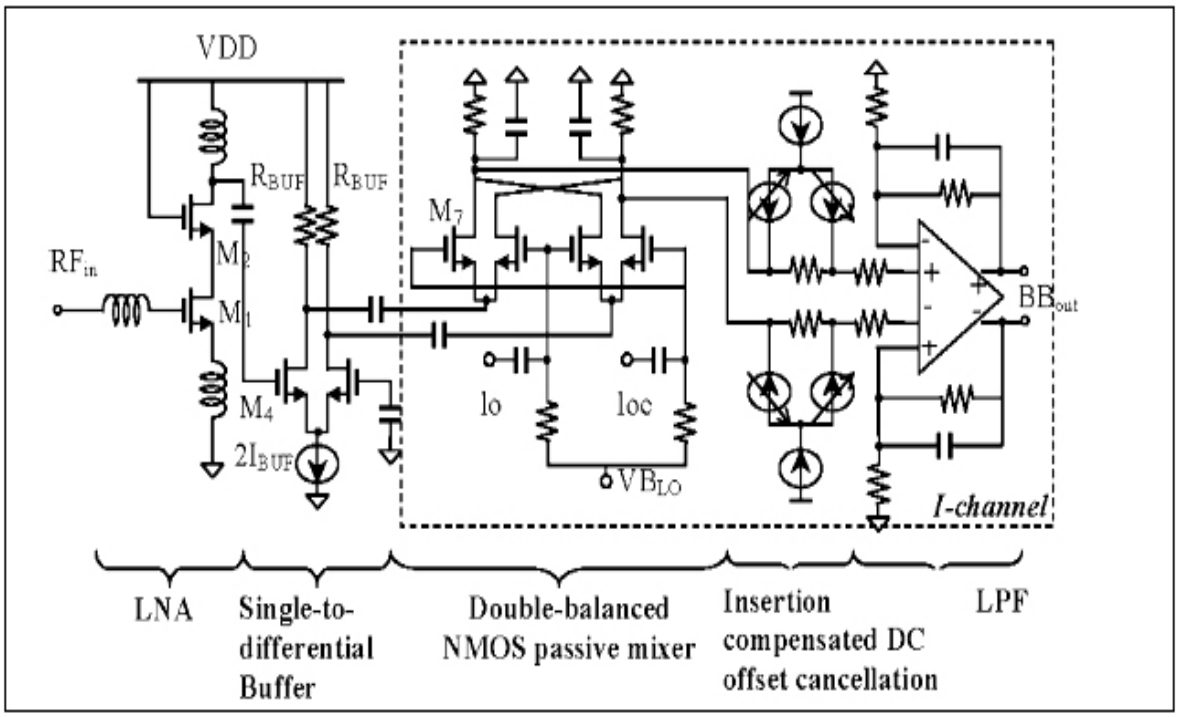


Figure 3.9 Low flicker-noise mixer with a passive configuration

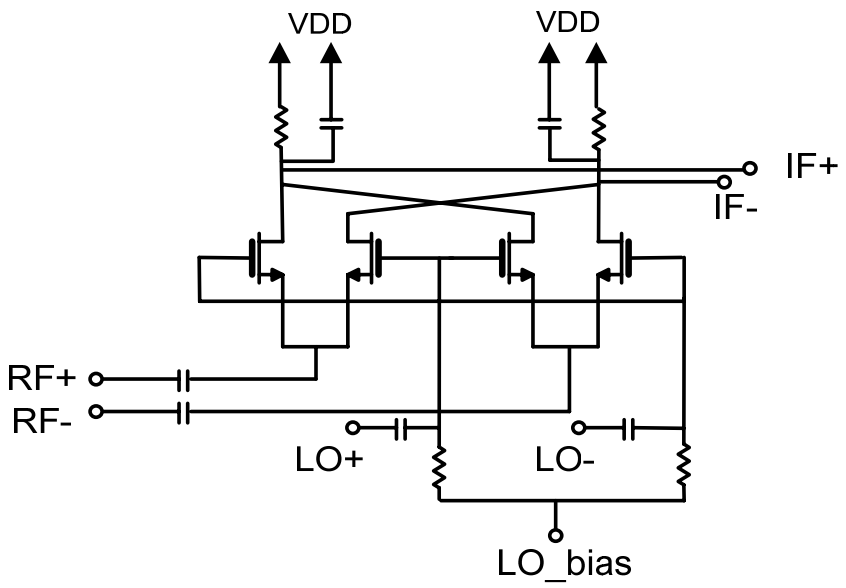


Figure 3.10 The schematic of a mixer with a passive configuration

Recently, the work in [23] achieved a positive conversion gain and very low flicker corner frequency (45 kHz) with an LO bias-shifting network that automatically tracks the dc offset and its circuit implementation is shown in Figure 3.9 and Figure 3.10.

Advantages –

- To obtain a very low flicker corner frequency is possible (45kHz).
- Low power and less die area than an active mixer.
- Less LO power required because it does not need a switching
- More easier implementation for DC offset cancellation.

Drawbacks –

- The conversion gain is lower than any conventional Gilbert-type active mixer.
- Not good isolation performance than any conventional Gilbert-type active mixer.

3.3 Low flicker-noise receiver front-end

The use of dynamic matching that was suggested by Motorola has improved the mixer's close-in noise performance by greatly reducing the contribution of flicker or 1/f noise. The dynamic matching is utilized to mitigate the effects of both component and device mismatches so this enhances overall circuit balance.

Switched biasing is proposed as a technique for reducing the 1/f noise in MOSFET's. Conventional techniques, such as chopping or correlated double sampling, reduce the effect of 1/f noise in electronic circuits, whereas the switched biasing technique reduces the 1/f noise itself. Whereas noise reduction techniques generally lead to more power consumption, switched biasing can reduce the power consumption. It exploits an intriguing physical effect: Cycling a MOS transistor from strong inversion to accumulation reduces its intrinsic 1/f noise. As the 1/f noise is reduced at its physical roots, high frequency circuits, in which 1/f noise is being upconverted, can also benefit.

The LNA and the RF mixer determine the upconversion of flicker noise. To suppress the 1/f noise generated by the LNA, the amplified signal can be capacitively coupled to the input device of the mixer. However, since the MOS transistors used in the LNA and the mixer have relatively small dimensions, their flicker-noise corner frequency may be as high as several megahertz (in case of 0.25μm CMOS device). Thus, the signal-to-noise ratio (SNR) may degrade considerably. The mixer is the most critical stage in the receiver chain in combating the flicker noise. In a conventional single balanced mixer, one faces a difficult tradeoff in choosing the proper biasing between switching quad and V/I converter. The switching quad devices exhibits lower flicker

noise if bias current can be reduced, while the V/I converter device requires a high biasing current to achieve a decent conversion gain and good linearity. In Razavi's work, a two-stage mixer is used where the V/I converter and the switching quad biasing currents can be independently optimized [2].

In the 5GHz direct down conversion 0.18μm CMOS transceiver by Razavi, a spot noise figure of 6.8 dB is measured at 5-MHz baseband signal frequency [2]. The flicker noise effect is shown at 1 MHz and below. According to the 802.11a standard, the first subcarrier of the OFDM signal starts at 150 kHz, where the noise figure is about 8 dB, which is still 2 dB better than the 802.11a standard noise figure assumption of 10 dB.

In the broadcom's 5GHz direct conversion 0.18μm CMOS receiver, the average NF across the band of interest (up to more than 10MHz) is maintained at about 4.0 dB. Also it is noted that the spot NF at the frequency of the lowest OFDM subcarrier (312KHz) is maintained at below 5dB. The flicker corner frequency is observed at about 400KHz.

In the STM's 5GHz direct conversion 0.13μm CMOS receiver, the NF of 3.5dB in the center of the band is maintained and a 1/f corner frequency of 200KHz is achieved [25]. Its key feature is current driven passive mixer with a low impedance load that achieves a low 1/f noise corner. By using the same design concepts as current driven passive mixer, 2.4GHz direct conversion 0.18μm CMOS receiver shows the NF of 4.4dB from 10KHz to 1.9MHz and a 1/f corner frequency of 70KHz [22].

CHAPTER IV

Design of Highly Linear Receiver Front-end

In this chapter, design methodologies, technical issues, and measurement results are discussed for a highly linear receiver front-end. To implement a highly linear receiver front-end, LNA and mixer are the key components as shown in Figure 4.1. LNA has to be very linear for multiband applications because it receives many signals directly from the antenna. In multiband RF applications, LNA is always in danger for saturation due to many interferers from other adjacent channels and high powered leaked signal from transmitter. Mixer also is one of key components for a highly linear receiver front-end because it generally receives larger signal than LNA.

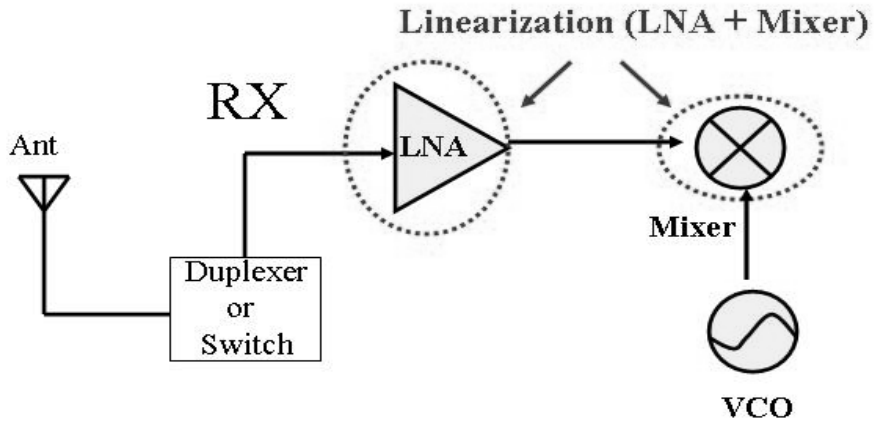


Figure 4.1 Highly linear direct conversion receiver architecture

4.1 Design consideration for highly linear LNA

The most efficient linearization method for CMOS LNA is the derivative superposition (DS) technique and it nulls the negative third-order derivative of the dc transfer characteristic (g_3) of the main FET which has a parallel connection with an auxiliary FET and it is biased near the weak inversion region with the positive g_3 [19]. The modified DS technique was proposed by adding two source-degeneration inductors in series to the conventional DS technique and it showed a measured IIP3 of +22dBm which is the highest IIP3 value among CMOS LNAs [6].

4.1.1 Single-ended LNA

The proposed LNA in this research is to use a NMOS as an IMD3 sinker as shown in Figure 4.2(a). In the conventional DS technique, the RF input is connected to both the main FET and the auxiliary FET. However, in this proposed LNA, the RF input is connected only to the main FET and the third-order transfer characteristics as follows

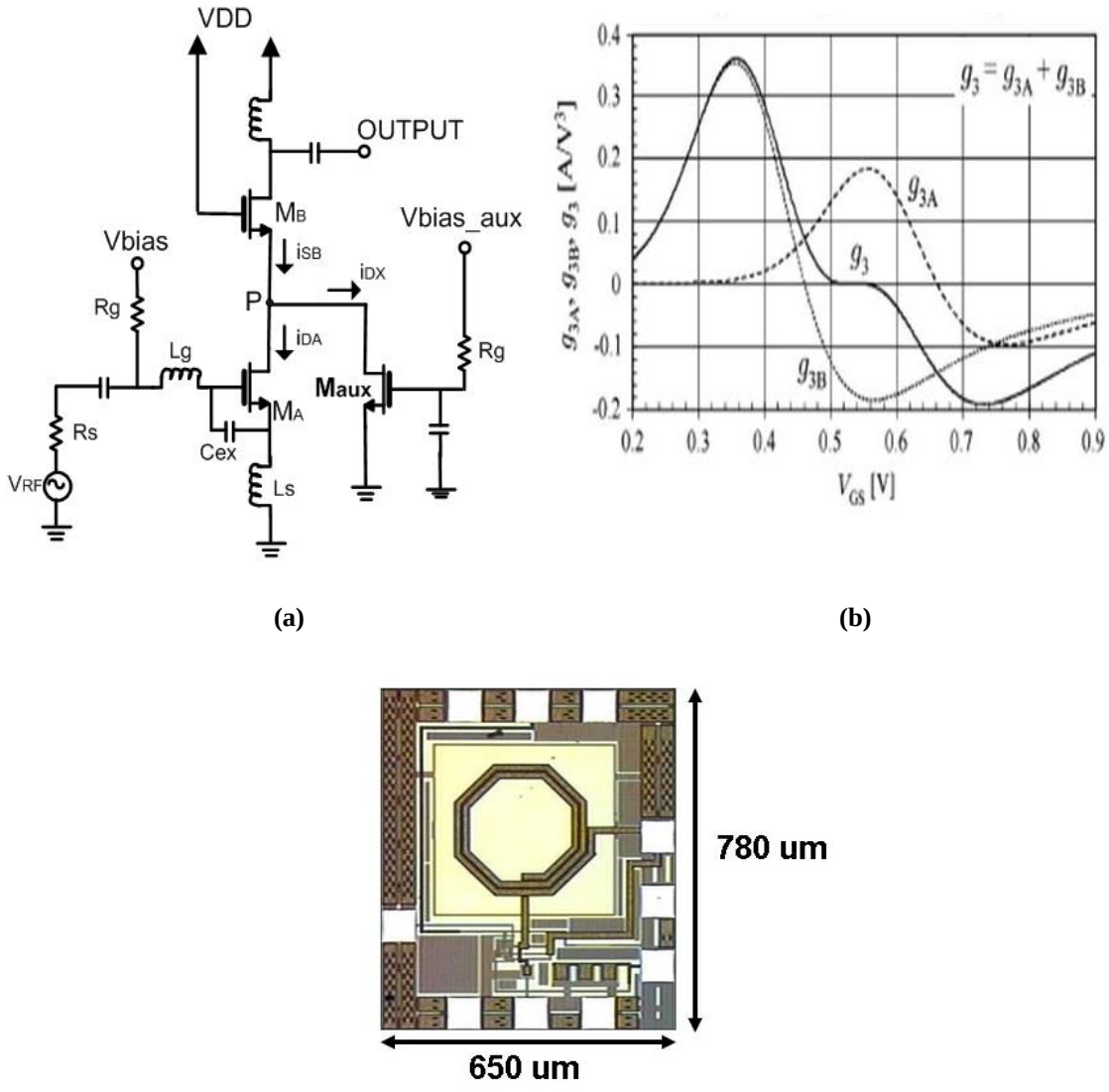
$$i_{sB} = i_{sA} + i_{dX} \approx (g_{1A} + x_1 g_{1X}) v_{gsA} + (g_{2A} + x_1^2 g_{2X}) v^2_{gsA} + (g_{3A} + x_1^3 g_{3X}) v^3_{gsA}. \quad (4.1)$$

Also, gm3's are composite third-order power-series coefficients defined by

$$g_{m3A} = \frac{\partial^3 i_{dA}}{\partial v^3_{gsA}}, g_{m3B} = \frac{\partial^3 i_{sB}}{\partial v^3_{gsA}}, g_{m3X} = \frac{1}{6}\frac{\partial^3 i_{sX}}{\partial v^3_{gsA}}.$$

(4.2)

The coefficient of the third term in (4.3) can be made zero by adjusting the gate bias of Maux and the size of MB and Maux. The g_{m3A} of the FET MA can be compensated by g_{m3C} of the folded NMOS Maux. Therefore, Maux can absorb the third-order nonlinearity generated by MA.



(a) **(b)**

(c)

Figure 4.2 (a) the proposed single-ended LNA (b) Third-order power series coefficients (c) Die photograph of the chip

Table 4.1 shows the simulation results and an IIP3 of 5.3dBm has been improved by the proposed technique. The IMD3 of the drain current of the M_A in Figure 4.2(a) is proportional to [6]

$$IIP_3 = \frac{4g_1{}^2\omega^2 LC_t}{3|\varepsilon|}$$

$$\varepsilon = g_3 - \frac{2g_2{}^2/3}{g_1 + \frac{1}{j2\omega_0 L_s} + j2\omega_0 C_t + Z_s(2\omega_0)\frac{C_t}{L_s}} \tag{4.3}$$

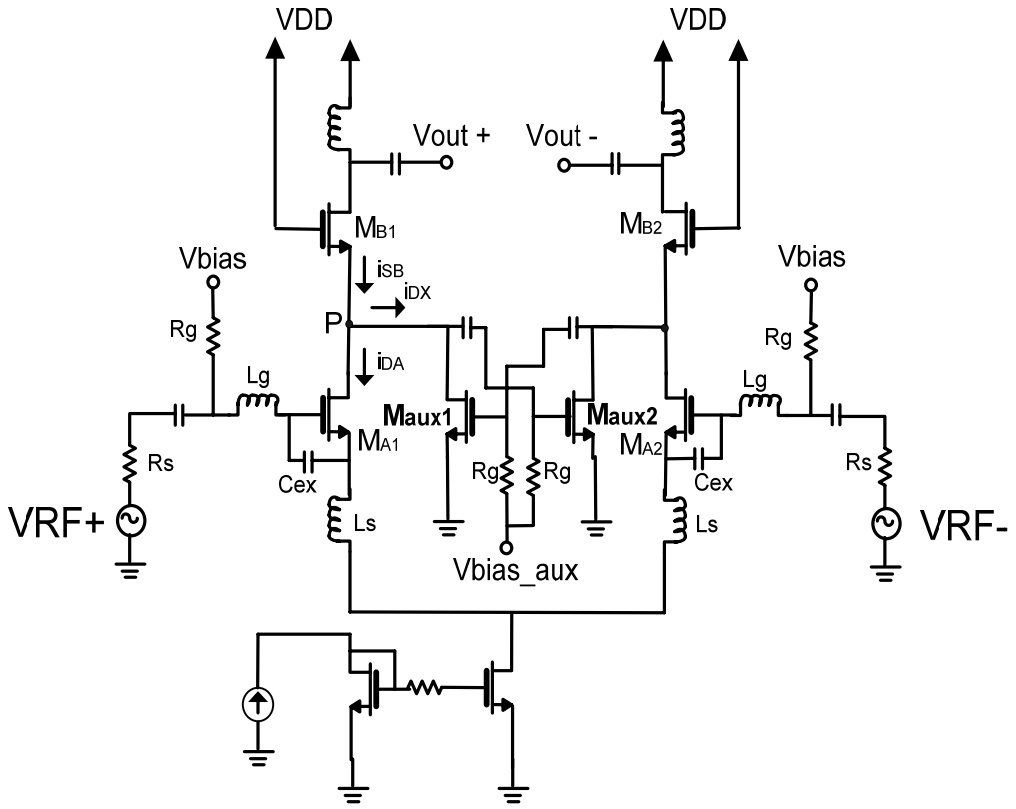
where $Z_s(2\omega_0) = R_s + j2\omega_0 L_g, C_t = C_{ex} + C_{gs}$.

Table 4.1 Simulated results of the single-ended LNA

Topology	IDC (mA)	**NF**	**IIP3 (dBm)**	**Gain**
Conventional cascade LNA	8	**1.2**	**3**	**16.5**
Proposed LNA	9.5	**1.5**	**8.3**	**13.5**

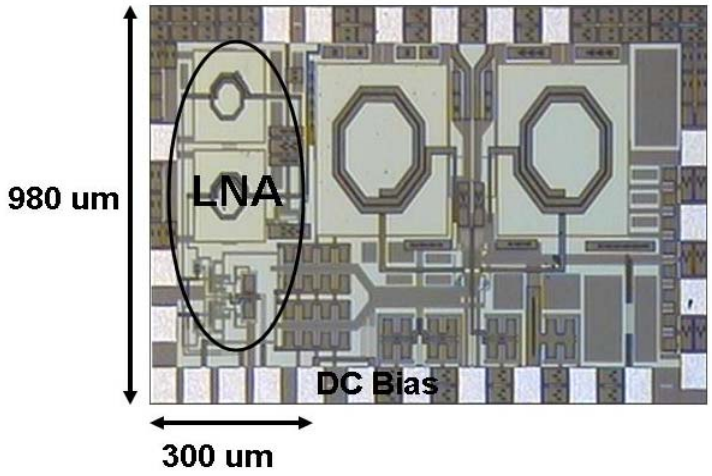
4.1.2 Differential LNA

In general, the output of LNA has to be differential because the Gilbert-type mixer has differential inputs. Otherwise, a single-to-differential balun circuit has to be placed between LNA and mixer to convert the single output of LNA with the differential output. However, a balun itself degrades the linearity of the receiver and consumes more power. Therefore, differential LNA has to be designed. The proposed differential LNA in this research is to use a NMOS as an IMD3 sinker as shown in Figure 4.3(a) and Figure 4.3(b) shows the die photograph of the chip.



(a)

Figure 4.3 (a) The differential LNA



(b)

Figure 4.3 Continued (b) Die photograph of the chip

The IMD3 of the drain current of the M_A in Figure 4.3(a) is proportional to

$$IIP_3 = \frac{4g_1^{\,2}\omega^2 LC_t}{3|\varepsilon|} \tag{4.4}$$

$$\varepsilon = g_3 - \frac{2g^2{}_2/3}{g_1 + \frac{1}{j2\omega_0 L_s} + j2\omega_0 C_t + Z_s(2\omega_0)\frac{C_t}{L_s}} \tag{4.5}$$

where $Z_s(2\omega_0) = R_s + j2\omega_0 L_g, C_t = C_{ex} + C_{gs}$

Table 4.2 Simulated results of the differential LNA

Topology	IDC (mA)	**NF**	**IIP3 (dBm)**	**Gain**
Conventional cascade LNA	15	**2.8**	**3**	**22**
Proposed LNA	15.8	**3.5**	**10**	**20.5**

4.2 Design consideration for highly linear Mixer

To implement a highly linear and low flicker-noise receiver, a mixer is a critical component. Therefore, the mixer has to have very highly linear and show good flicker-noise performance. High linear mixers afford more gain at LNA stage, which improves the system noise figure and relaxes the flicker noise margin especially for CMOS design. Recently, continued scaling of CMOS technology enables the successful design of the high gain and low noise mixer with low power consumption. However, the linearity of CMOS mixers has not benefited by the technology evolution and therefore efficient linearization techniques are essential. Compared to CMOS mixers, several linearization methods have been proposed for high linear CMOS LNAs. One of the successful linearization techniques is the derivative superposition (DS) technique [1,2]. This method cancels the negative third order nonlinearity of the main FET's dc transfer characteristic (g_3) by paralleling the auxiliary FET biased near the weak inversion region with the positive g_3. The same approach has been used for the linearization of the folded switching mixer with a resonant load [2]. However, according to simulation, the conventional DS approach is not successful in the linearization of the Gilbert cell switching mixer. A single-balanced active CMOS mixer is composed of a transconductance stage and a switching pair. The total mixer third-order intermodulation (IM3) at low frequencies is approximated by

$$IM_3 \approx \frac{3}{4}\left(\frac{a_3}{a_1} + \frac{b_3}{b_1}a_1^2\right)v_{in}^2 \tag{4.6}$$

, where v_{in} is the amplitude of each input tone in the two tone test and a_1, a_3 are linear and third order nonlinear coefficients of the transconductance stage [3]. The coefficients b_1 and b_3 in (4.6) are the linear and third order nonlinear current conversion coefficients of the switching stage from RF to IF defined in [3]. Then, the condition for canceling IM3 is given by

$$a_3 = -\frac{b_3}{b_1} a_1^3 . \tag{4.7}$$

The condition (4.7) means that the switching stage intermodulation can be cancelled by the optimally controlled transconductance stage nonlinearity. The sign of a_1 and b_1 is obviously positive, but the sign of b_3 needs to be investigated. According to the numerical calculation following the methods in [3], usual switching pair design results in the negative b_3 as shown in Figure 4.4. Therefore, canceling the IM3 requires the positive third order nonlinearity at the transconductance stage with an optimum transconductance gain, which can be achieved through the proper sizing and biasing of the main and auxiliary FETs. It can be called as a positive DS technique.

The condition (4.7) is derived assuming memoryless devices and valid at low frequencies. At RF, due to the several parasitic capacitances of FETs, rigorous analysis relies on time-varying Volterra series expansion, but the final results are too complicated for practical use. Instead, the harmonic balance (HB) analysis can be used to investigate the behavior of the intermodulation distortion at RF. According to simulation at RF, it is found that the third order intermodulation generated by the switching FETs deviates from the out-of-phase relation with the fundamental current while the transconductance stage maintains the similar phase relation as it shows at low frequencies. Therefore, the

positive third order intermodulation of the transconductance stage can not effectively cancel the intermodulation of the switching stage due to the phase mismatch at high frequencies. Fortunately, the phase of the switching stage intermodulation can be controlled by adding an inductor at the tail of the switching stage. The other node of the inductor can be ac-grounded for a single balanced mixer or connected to the other switching tail for a double balanced mixer (DBM) as shown in Figure 4.5. HB simulation confirms the phase change of the intermodulation current of the switching stage according to the change of the inductance as shown in Figure 4.5. These simulation results are obtained for a single balanced mixer composed of a real switching FET pair with a parasitic tail capacitance and an ideal linear transconductance stage. It is found that there is an optimum inductance value which restores the 180° phase relation between the fundamental and third order intermodulation currents generated by the switching stage. Therefore, it is possible to accomplish the IM3 reduction by using the positive DS technique at the transconductance stage and adding the tail inductor for the phase match. Though the tail inductor has been introduced to improve the third order nonlinearity in [4], the linearization mechanism is completely different from this work.

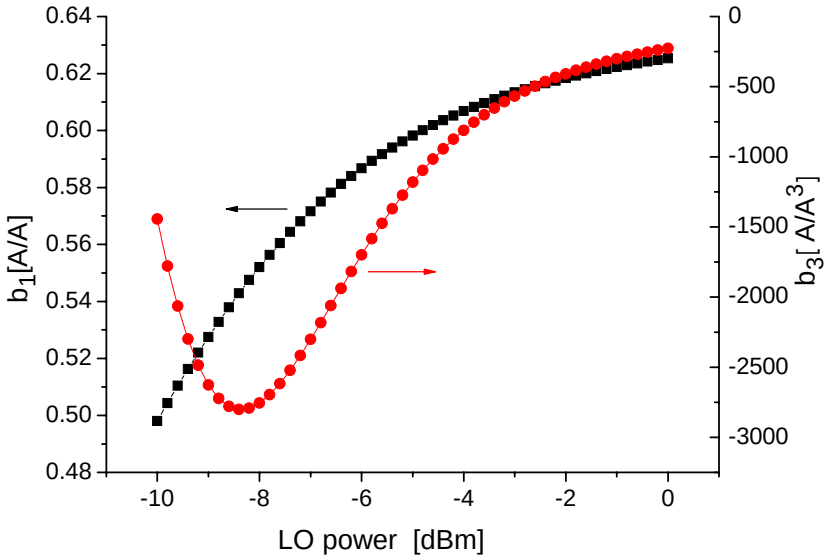


Figure 4.4 Variation of sign and magnitude of b_3 versus LO drive level

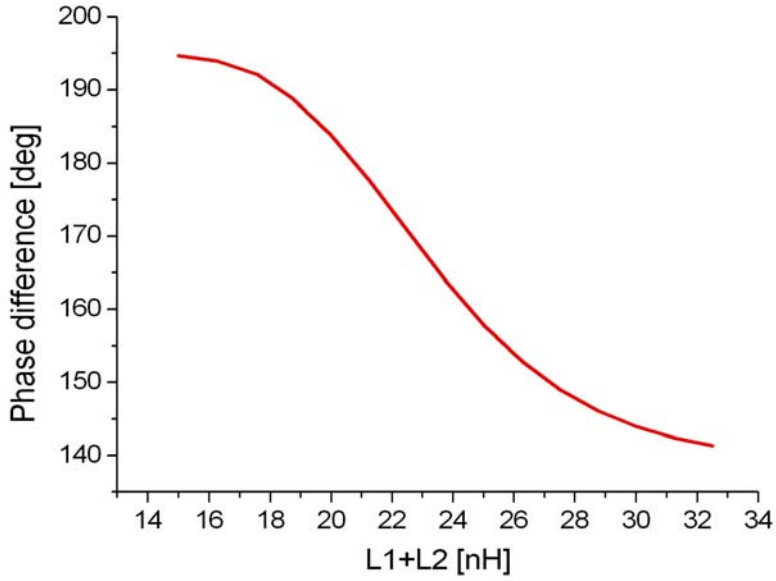
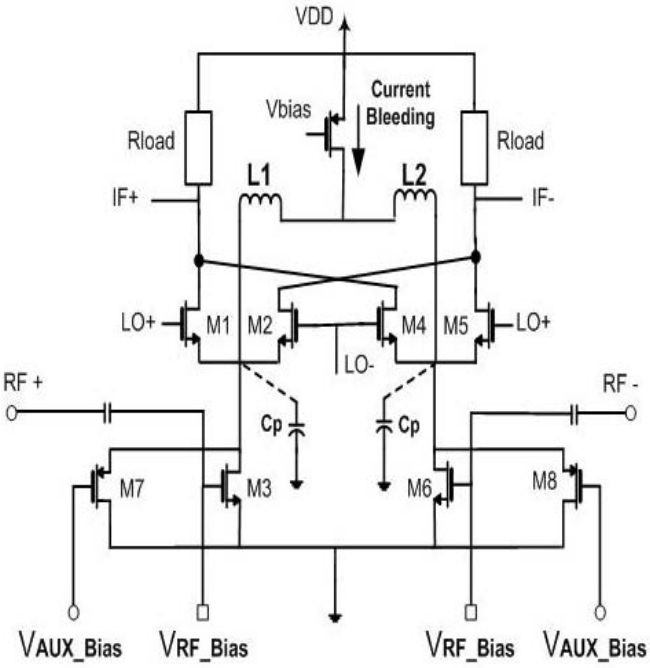


Figure 4.5 Phase difference between the fundamental and intermodulation currents of the switching stage at the IF output versus the value of the tail inductor L1+L2

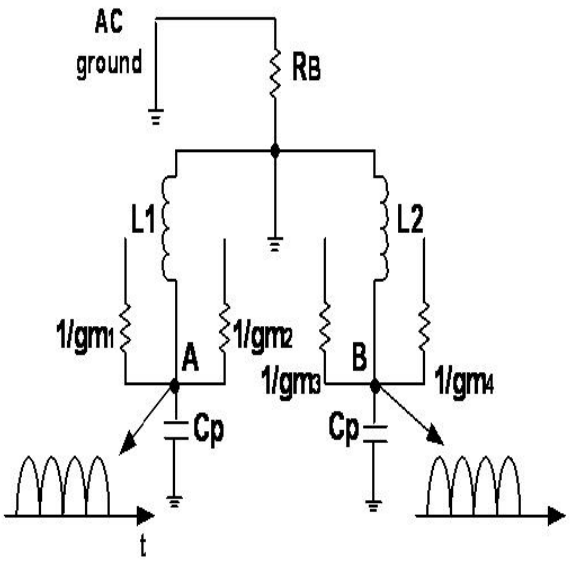
4.2.1 Highly linear and low flicker noise mixer using DS technique with separate RF bias voltage

According to the results of the preliminary research activities, the static current bleeding technique with two resonating inductors is an attractive method to decrease the effect of flicker noise by both the direct mechanism and the indirect mechanism. Figure 4.6(a) shows the proposed highly linear and low flicker-noise mixer implemented by incorporating a double-balanced Gilbert-type configuration, the RF leakage-less static current bleeding technique, the resonating technique for the tail capacitance, and the derivative superposition (DS) linearization technique for the RF transconductance transistors. Two inductors are connected to the source node of the LO switches to decrease flicker noise and simultaneously to improve the IIP2 performance of the mixer. Because the second-order inter-modulation components due to odd as well as even LO harmonics add at the mixer output. Also, amplitude and phase of each component depends on the bias current of the LO switching pairs and the tail capacitance.

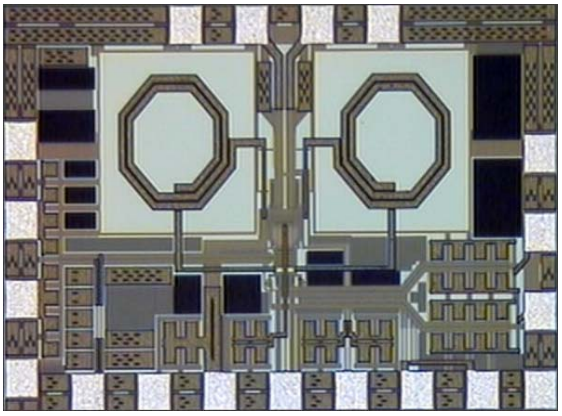
Two auxiliary transistors (M7 and M8) are used to improve the IIP3 performance of the mixer and the bias voltage of the auxiliary transistors (M7 and M8) should be optimized with the sizes of these two transistors to properly implement the derivative superposition (DS) linearization technique. Table IV shows the simulation results on the proposed mixer. The IIP2, IIP3, and flicker noise performance are improved by 10dB, 18dB, and 760kHz, respectively.



(a)



(b)



(c)

Figure 4.6 (a) Highly linear and low flicker noise mixer (b) Small signal model (c) Die photograph of the chip

Table 4.3 Simulated results of the proposed mixer

Topology	IDC (mA)	**IIP2 (dBm)**	**IIP3 (dBm)**	**Flicker Corner Freq. (kHz)**
Conventional Gilbert-type Mixer	4	**55**	**0**	**850**
Proposed Mixer	4	**65**	**18**	**90**

All measurements were performed using an on-wafer probe station. The variations of conversion gain with LO power for the proposed mixer is measured and plotted in Figure 4.7. Conversion gain is also varied as the resonating frequency is changed. This means that conversion gain is maximized under resonant condition.

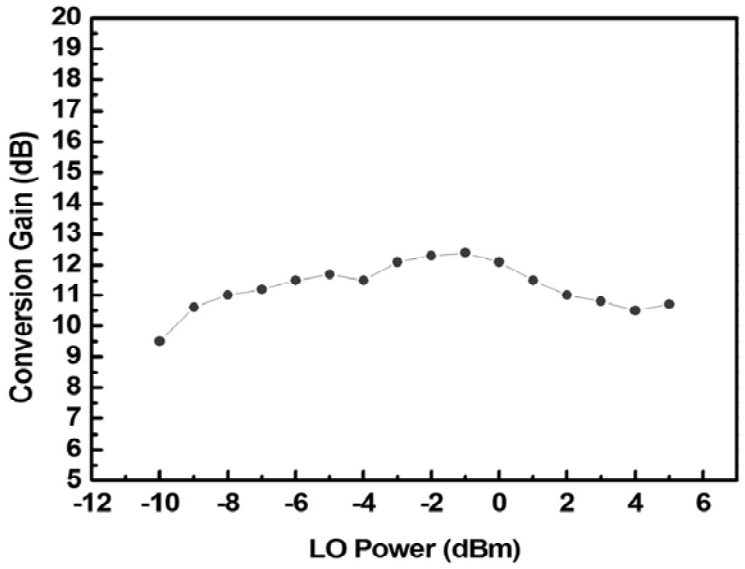


Figure 4.7 Measured conversion gain variation with LO power

The noise figure of the proposed mixer is found to be 10.1 dB at 1 MHz and above. At the rated RF frequency of 5.2 GHz, the measured conversion gain for the mixer with two resonating inductors is 12.2 dB and this gain is obtained when the balanced LO signal powers are at -1 dBm. The mixer has a measured input 1dB compression point of -6 dBm and an IIP3 of 15 dBm which is the highest IIP3 value ever reported using a CMOS active mixer based on experimental results. It is shown in Figure 4.8. The LO to RF isolation is 38.7 dB.

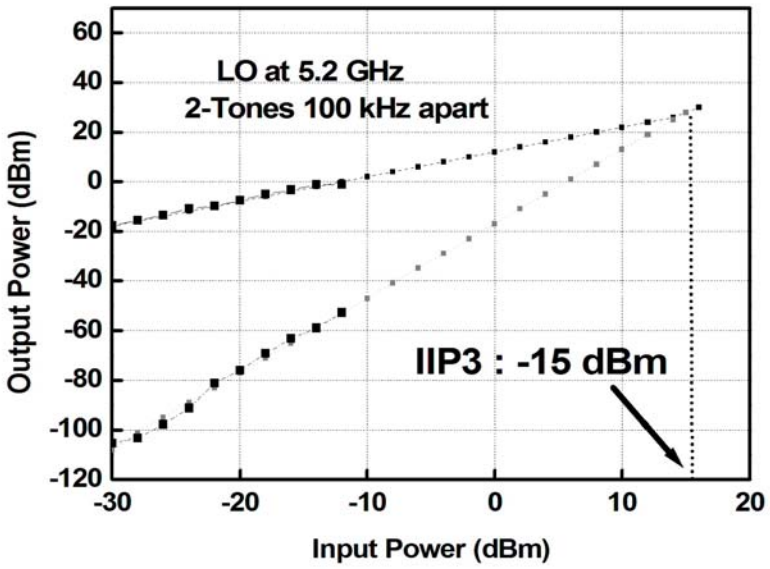


Figure 4.8 Measured Input third order intercept point of the mixer

Figure 4.9 shows output noise power spectral density which was measured on both HP 4395A Low-frequency Spectrum Analyzer and Agilent 35670A Dynamic Signal Analyzer for more accurate measurement. Also, as shown in Figure 4.10, the measured flicker corner frequency is 130kHz.

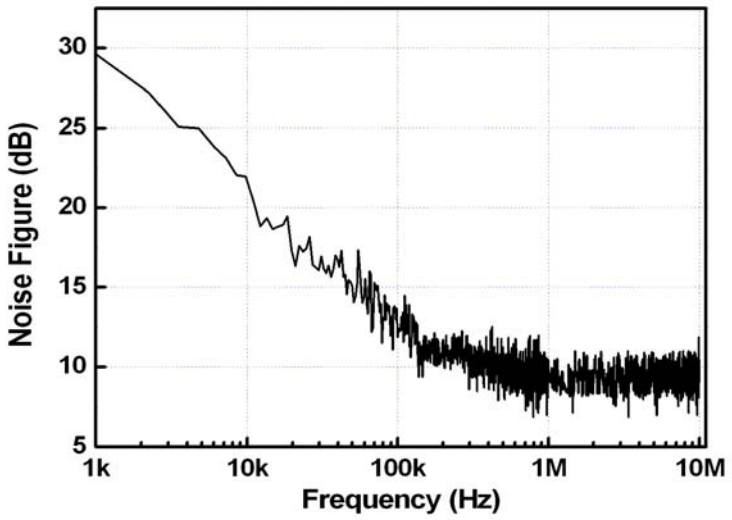


Figure 4.9 Measured noise figure of the mixer

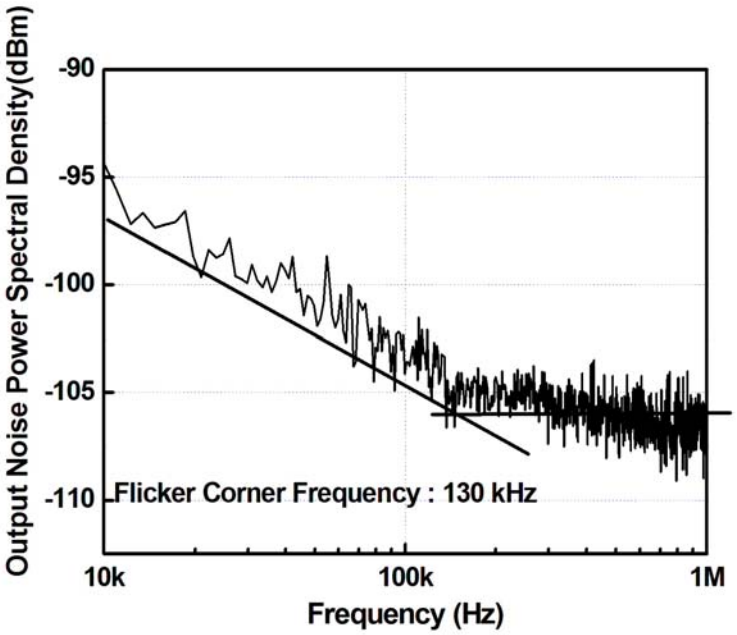
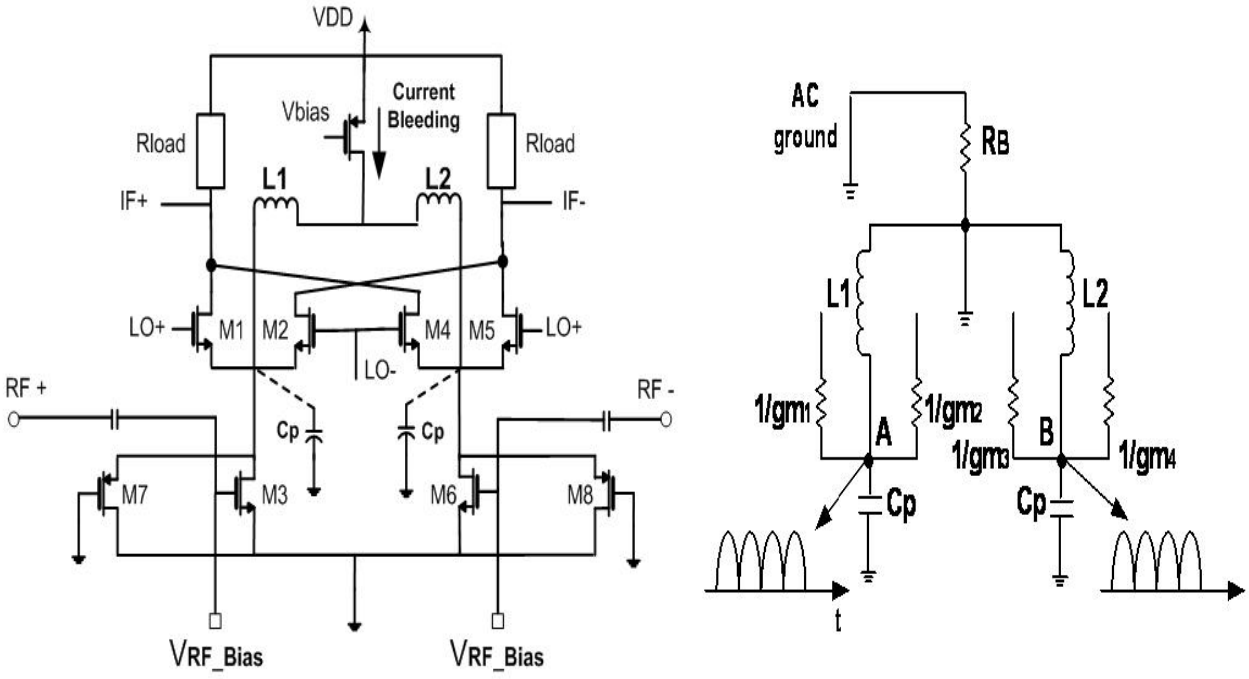


Fig. 4.10 Measured flicker corner frequency of the mixer.

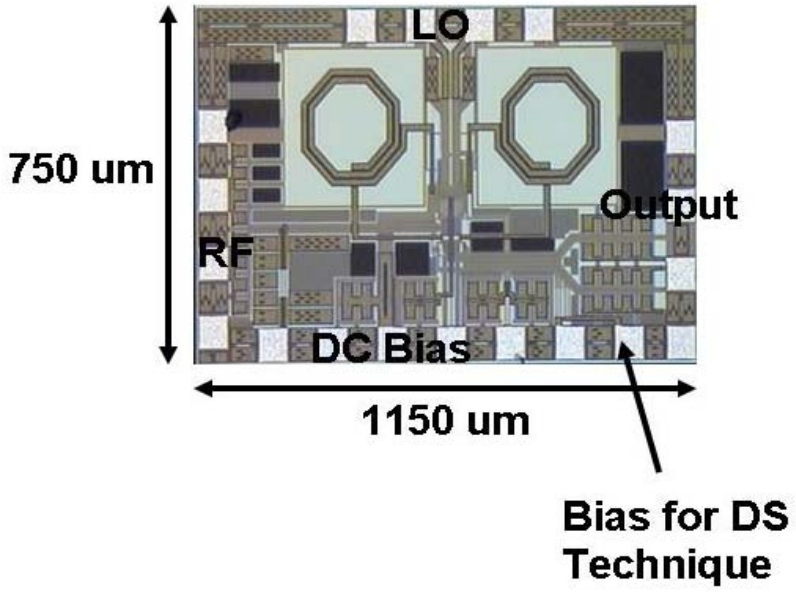
4.2.2 Highly linear and low flicker-noise mixer using DS technique with grounded RF bias voltage

Figure 4.11(a) shows another proposed highly linear and low flicker-noise mixer implemented by incorporating a double-balanced Gilbert-type configuration, the RF leakage-less static current bleeding technique, the resonating technique for the tail capacitance, and DS linearization technique for the RF transconductance transistors. However, the bias voltage for the RF stage to implement the DS technique is connected to ground. The optimum bias voltage for the DS technique can be controlled by adjusting the LO bias voltage. Therefore, this mixer can reduce one bias voltage and it is less sensitive to bias voltage than conventional DS technique.



(a) **(b)**

Figure 4.11 (a) Highly linear and low flicker noise mixer (b) Small signal model



(c)

Figure 4.11 Continued (c) Die photograph of the chip

Table 4.4 shows the simulation results on the proposed mixer. The IIP2, IIP3, and flicker noise performance are improved by 12dB, 19dB, and 765kHz, respectively.

Table 4.4 Simulated results of the proposed mixer

Topology	IDC (mA)	**IIP2 (dBm)**	**IIP3 (dBm)**	**Flicker Corner Freq. (kHz)**
Conventional Gilbert-type Mixer	4	**55**	**0**	**850**
Proposed Mixer	4	**67**	**19**	**85**

The variations of conversion gain with LO power for the proposed mixer is measured and plotted in Figure 4.12. The noise figure of the proposed mixer is found to be 10.4 dB at 1 MHz and above. At the rated RF frequency of 5.2 GHz, the measured conversion gain for the mixer with two resonating inductors is 12.9 dB and this gain is obtained when the balanced LO signal powers are at -1 dBm. The mixer has a measured input 1dB compression point of -6.7 dBm and an IIP3 of 15.3 dBm which is the highest IIP3 value ever reported using a CMOS active mixer based on experimental results. It is shown in Figure 4.13. The LO to RF isolation is 35.3 dB. Figure 4.14 shows output noise power spectral density which was measured on both HP 4395A Low-frequency Spectrum Analyzer and Agilent 35670A Dynamic Signal Analyzer for more accurate measurement.

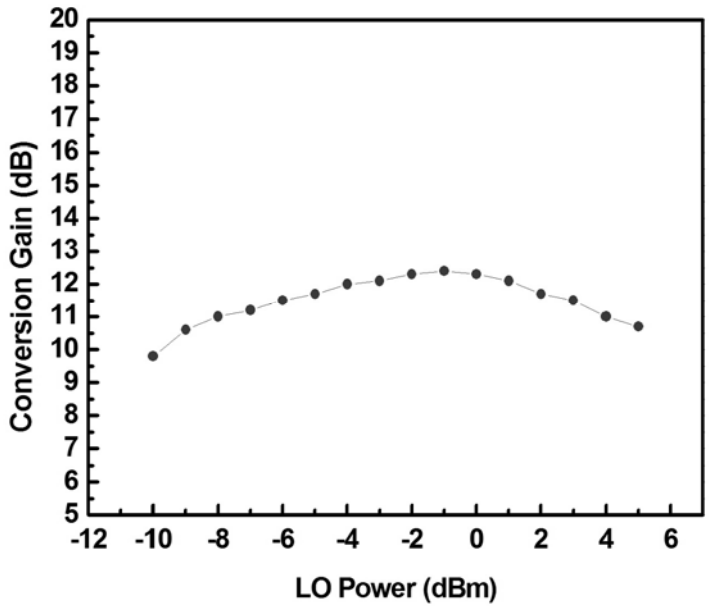


Figure 4.12 Measured conversion gain variation with LO power

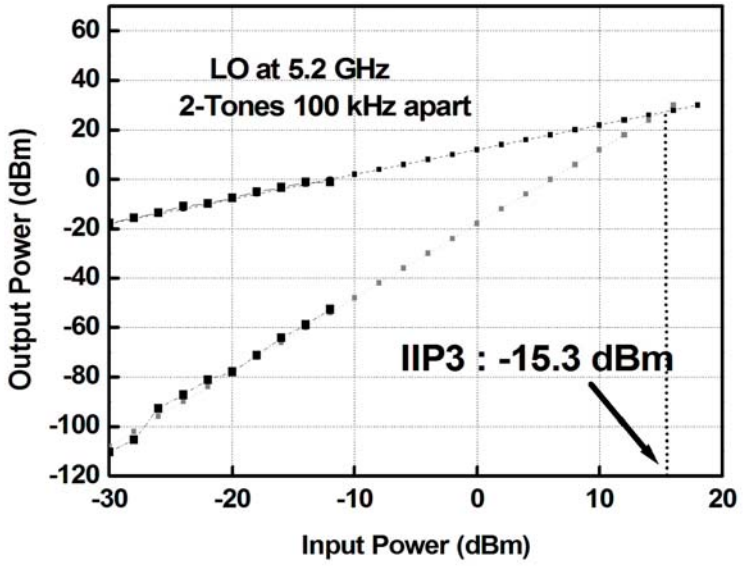


Figure 4.13 Measured Input third order intercept point of the mixer

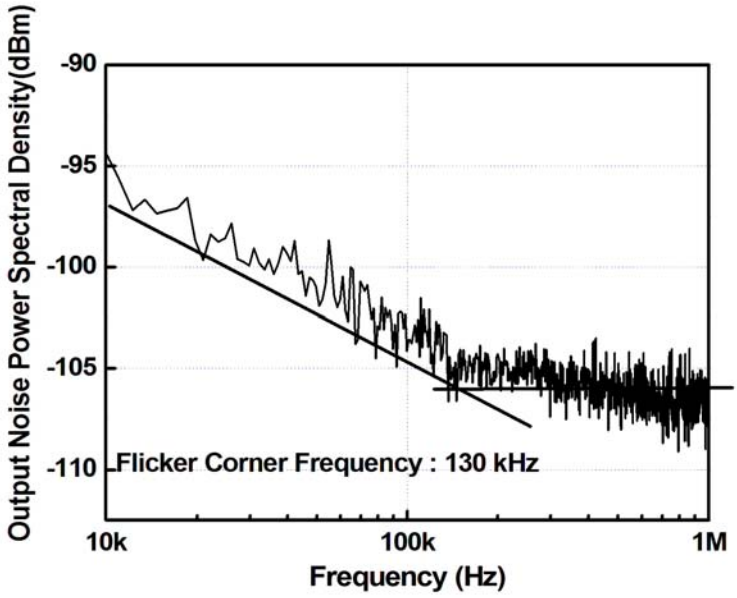
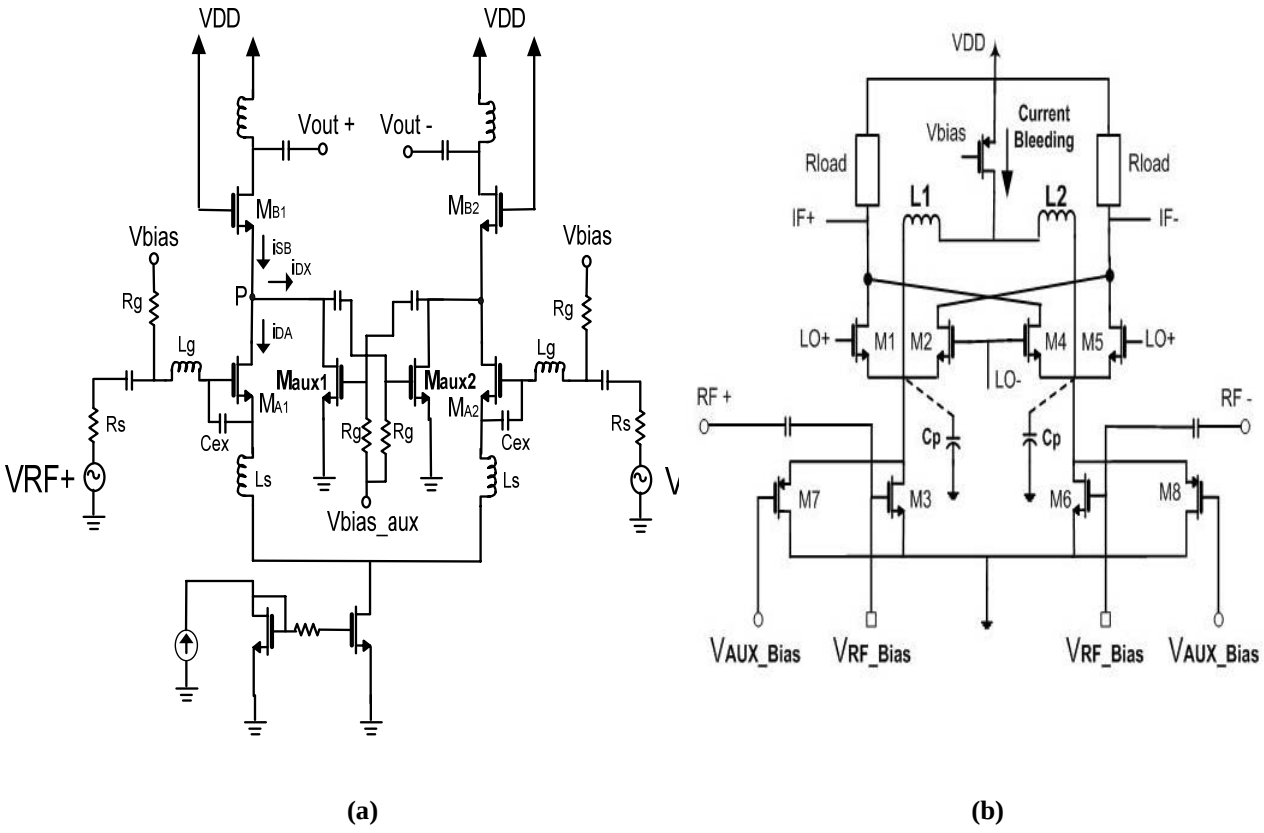


Figure 4.14 Measured flicker corner frequency of the mixer

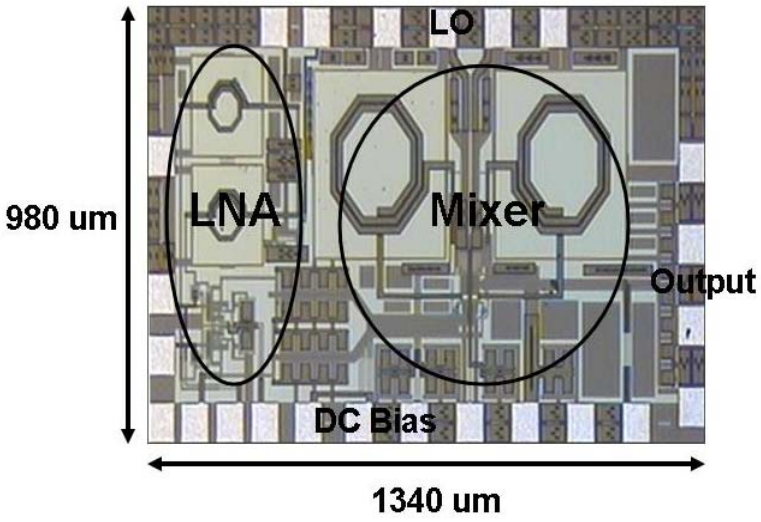
4.3 Design consideration for highly linear receiver front-end

To implement a highly linear and low flicker-noise direct conversion receiver front-end, a highly linear differential LNA using a NMOS IMD sinker has been fabricated and measured. Two capacitors were used to compensate the phase difference between the drain node of M_{A2} and the gate node of M_{aux1} as shown in Figure 4.15(a). Also, a highly linear and low-flicker noise mixer has been fabricated using a static current bleeding technique, two resonating inductors, and DS technique with grounded RF bias as shown in Figure 4.15(b).



(a) **(b)**

Figure 4.15 (a) Highly linear LNA (b) Highly linear and low flicker-noise mixer



(c)

Figure 4.15 Continued (c) Die photograph of the receiver chip

Figure 4.15(c) shows the die photograph of the fabricated receiver front-end chip and Table 4.5 shows the measured results of the proposed receiver front-end.

Table 4.5 Measured results of the highly linear receiver front-end

	Performance of the highly linear receiver
Gain	25 dB
Noise figure	2.5 dB
Operating bandwidth	5.2GHz
Input return loss	Less than -15dB
Input P1dB	-6dBm
IIP3	5dBm
IIP2	35dBm
Power consumption	9mA from 1.8V supply
Technology	0.18um TSMC CMOS

CHAPTER V

Design of Low Flicker-Noise Receiver Front-end

The objectives of this chapter are:

- To design and check the feasibility of the low flicker-noise mixers.
- To implement initial techniques to decrease flicker noise of the receiver.
- To identify the possible issues with the implementation of a low flicker-noise receiver in CMOS technology.
- To identify the trade-offs between improved flicker noise performance, conversion gain, die-area, power consumption, etc.

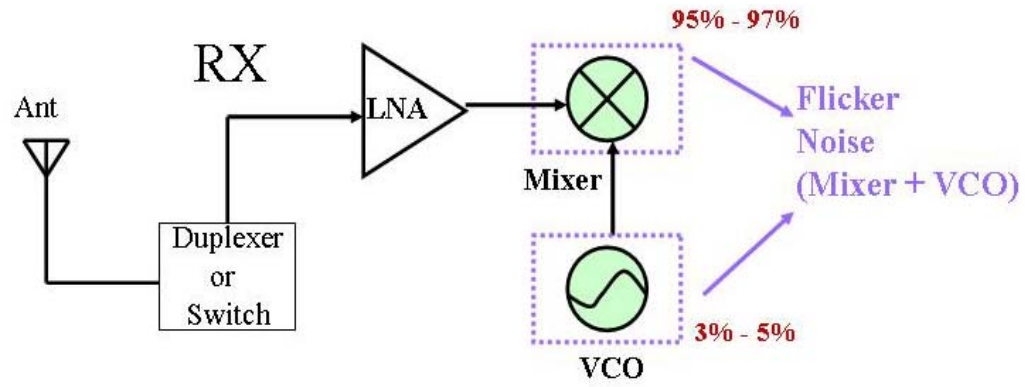


Figure 5.1 Diagram of the low flicker-noise receiver

Mixer is the key block to implement a highly linear and low flicker-noise direct conversion receiver as shown Figure 5.1. The design feasibility of both the highly linear

and low flicker-noise receiver has been checked for C-band application. The trade-offs between flicker noise performance on one hand, and conversion gain and power consumption on the other, have been identified for further investigation. Also, simulation results to decrease flicker noise by using harmonic tuned VCO are discussed. The results of the individual research contributions are discussed as follows.

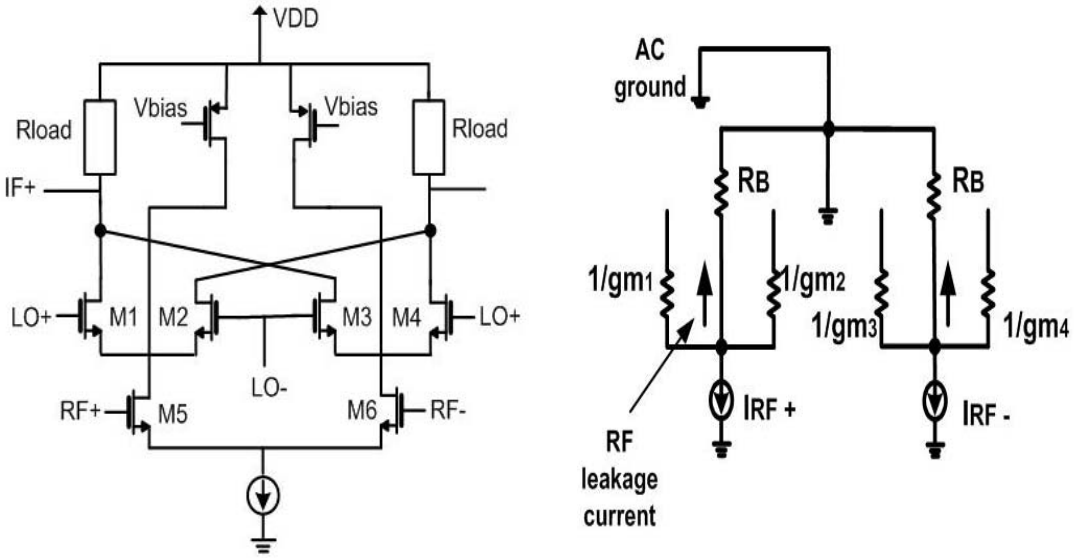
5.1 Design consideration for low flicker-noise mixer

5.1.1. Low Flicker Noise Mixer with Static Current Bleeding Technique

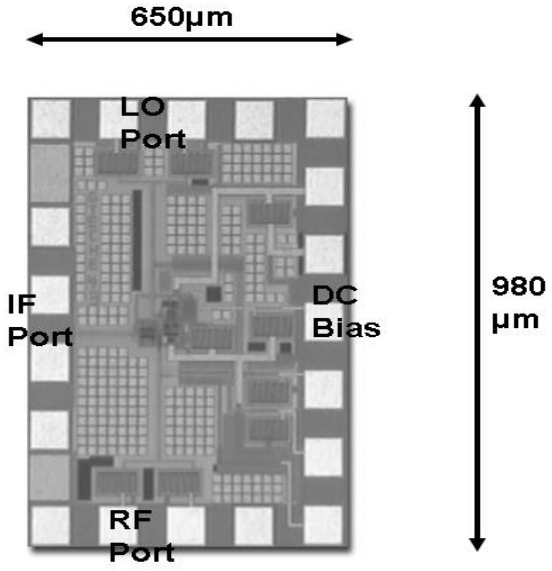
In general, increasing the bias current of the RF transconductance stage makes higher gain and better linearity possible, but a larger LO switching current causes voltage headroom issue. Therefore, as shown in Figure 5.2(a), the static current bleeding technique is implemented by using two PMOSFETs to reduce the bias current of the LO switches [4].

A. Design of Low Flicker Noise Mixer with Static Current Bleeding Technique

If the bias current of the LO switches is decreased, the output flicker noise current generated by the direct mechanism can be minimized. Figure 5.2(a) shows a double-balanced Gilbert-type mixer with current bleeding circuits. The mixer comprises an RF input transconductance stage, LO switches, output loads, and PMOS current bleeding circuits.



(a) **(b)**



(c)

Figure 5.2 (a) Circuit diagram of the Gilbert-type mixer with the static current bleeding (b) Small signal model (c) Die photograph of the chip

As shown in Figure 5.2(b), from (3.6) and (3.7), by current division,

$$I_{LO} = \frac{R_B}{\frac{1}{g_{m1}(t)+g_{m2}(t)} + R_B} \times \left[\frac{g_{m1}(t)-g_{m2}(t)}{g_{m1}(t)+g_{m2}(t)} \right] \times i_{RF}$$
$$= \frac{R_B \left[g_{m1}(t)-g_{m2}(t) \right]}{1+R_B \left[g_{m1}(t)+g_{m2}(t) \right]} \times i_{RF}. \quad (5.1)$$

As can be seen from (5.1), some RF current flows into the bleeding circuit by current division and it decreases conversion gain. On the other hand, the output noise current of LO switches is decreased as the bleeding current is increased. If the amount of the bleeding current is increased, the bias current of the LO switches is decreased. Then, as we can see from (3.9), the noise current by the direct mechanism is decreased. However, there are a few drawbacks with the conventional current bleeding technique. As the bias current of the LO switches is reduced, the impedance of the LO switches as seen from the RF stage is increased. Therefore, as shown in Figure 5.2(b), more RF leakage current flows into the bleeding circuit, which decreases conversion gain. It also allows more RF current to be shunted by the tail capacitance. To solve this drawback, the dynamic current injection method has been proposed [21]. The main idea of the dynamic current injection method is to inject current at only the switching event by using a control circuit [21]. Even though the dynamic injection is a good method to replace the conventional current bleeding technique, there are a few drawbacks. It shows a very low conversion gain which is similar to passive mixers, and also it may require high LO voltage swing to turn on and off the PMOS control circuit.

The main ideas in this preliminary research to design low flicker noise CMOS mixers are related to the following: how to reduce the bias current of LO switches, and

how to reduce the tail capacitance, which makes it possible to reduce flicker noise generated by the indirect mechanism. Both ideas should be considered simultaneously without sacrificing mixer bandwidth and linearity performance. First of all, the static current bleeding technique as shown in Figure 5.2(a) has been used to reduce the bias current of the LO switches.

B. Mixer Performance Summary

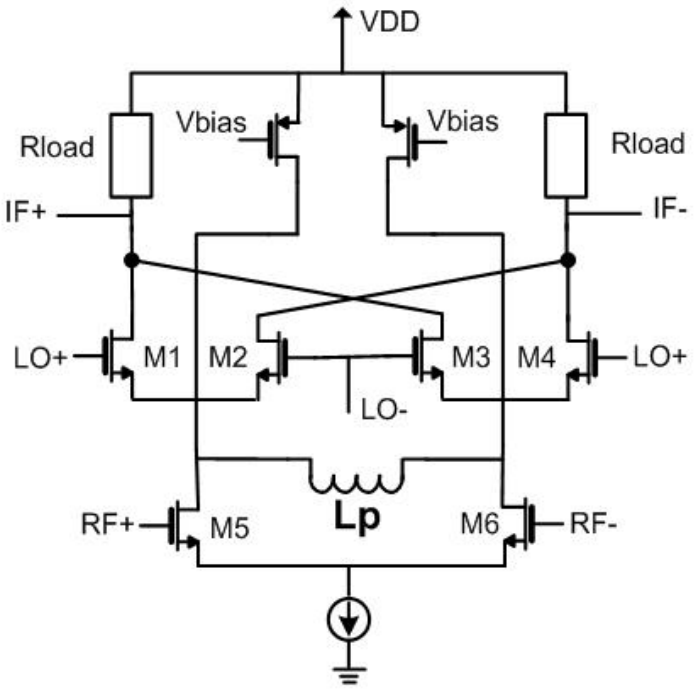
By using the Gilbert-type mixer with the static current bleeding technique, a measured conversion gain of 10dB and a flicker corner frequency of 550kHz has been achieved. The flicker corner frequency has been improved by 350kHz compared to the conventional Gilbert-type mixer. Detailed measurement results are compared and summarized in Section 5.4.

5.1.2. Low Flicker Noise Mixer with Static Current Bleeding Technique and One Resonating Inductor

Even if the current bleeding technique can reduce the bias current of the LO switches, flicker noises are still generated by the indirect mechanism. The main source of flicker noise by the indirect mechanism is the tail capacitance at the node between the LO switching pairs and the RF input transistors. Therefore, the tail capacitance, Cp, is still needed to be reduced.

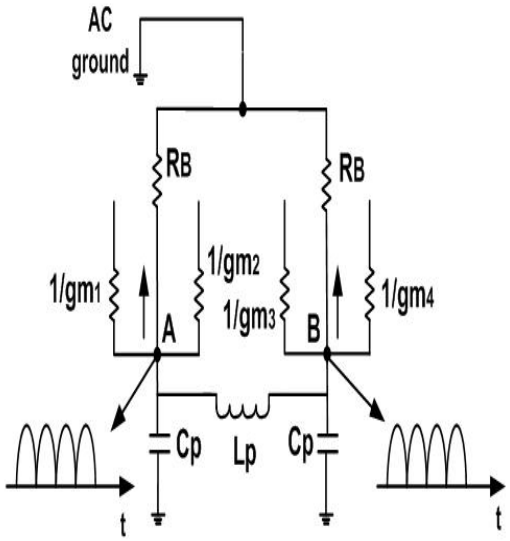
A. Design of a Low Flicker Noise Mixer with Static Current Bleeding Technique and One Resonating Inductor

The best way to reduce the tail capacitance is to minimize the size of the LO switches and RF transcondutance stages. However, CMOS transistors suffer from high intrinsic flicker noise, which is inversely proportional to the WL of the device. Therefore, one inductor, Lp, is connected between the common source node of the LO switches, as shown in Figure 5.3(a), to resonate the tail capacitance out, and the conversion gain and flicker noise performance are improved simultaneously under resonant condition.

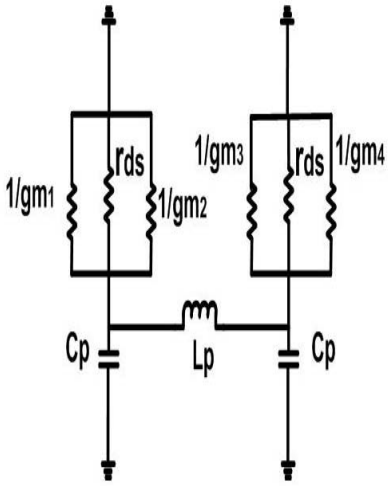


(a)

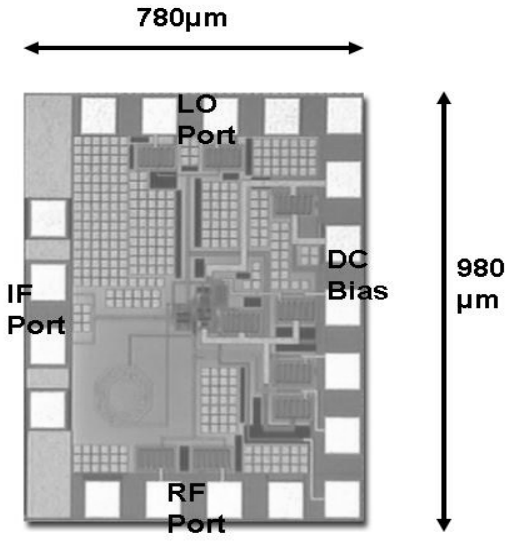
Figure 5.3 (a) Circuit diagram of the mixer with the static current bleeding and one resonating inductor



(b)



(c)



(d)

Figure 5.3 Continued (b) Small signal model (c) Simplified small signal model (d) Die photograph of the chip

Nonetheless, there is one drawback on the current bleeding technique with one resonating inductor. As we can see from Figure 5.3(b), some RF current can still flow into the current bleeding circuit, which decreases the conversion gain. By resonating the tail capacitance with Lp, the impedance at node A looking into Cp can be high enough to protect some RF current from being shunted by the tail capacitance. Figure 5.3(c) shows a simplified model which consists of a parallel RLC resonator. More detailed analysis on the parallel RLC resonator is done in Section 5.1.3.

B. Mixer Performance Summary

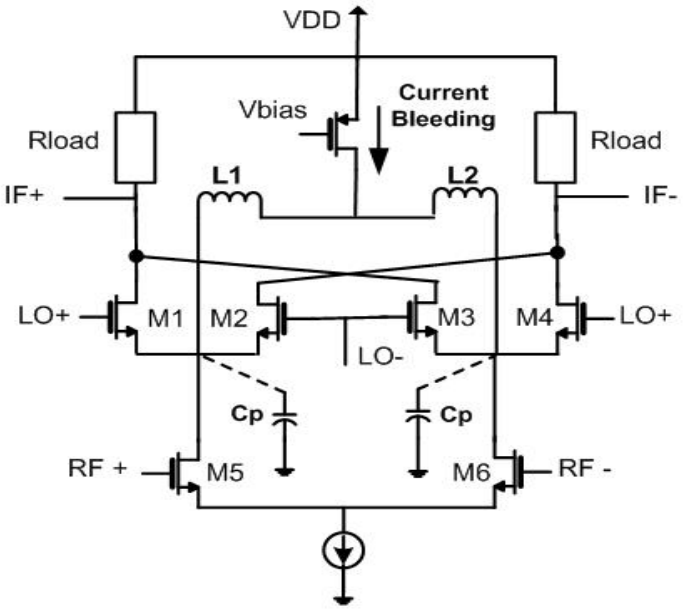
By using the Gilbert-type mixer with the static current bleeding technique and one resonating inductor, a measured conversion gain of 13dB and a flicker corner frequency of 180kHz has been achieved. The flicker corner frequency has been improved by 720kHz compared to the conventional Gilbert-type mixer. Detailed measurement results are compared and summarized in Section 5.4.

5.1.3. Low Flicker Noise Mixer with Static Current Bleeding Technique and Two Resonating Inductors

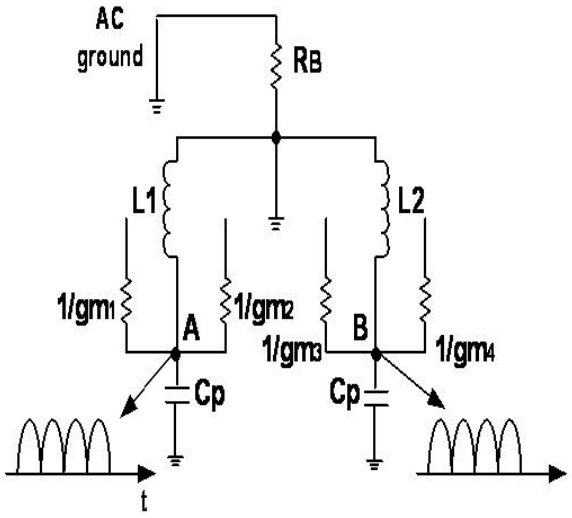
A. Design of a Low Flicker Noise Mixer with Static Current Bleeding Technique and Two Resonating Inductors

The final approach is to use the current bleeding technique with two inductors connected between the common source node of the LO switches and the PMOS as shown

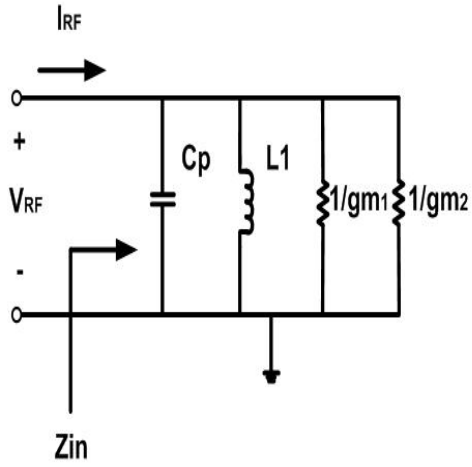
in Figure 5.4(a). Therefore, two inductors (3.3nH each) are connected to the PMOS device to resonate the tail capacitance out, and the conversion gain and flicker noise performance are improved simultaneously under resonant condition.



(a)

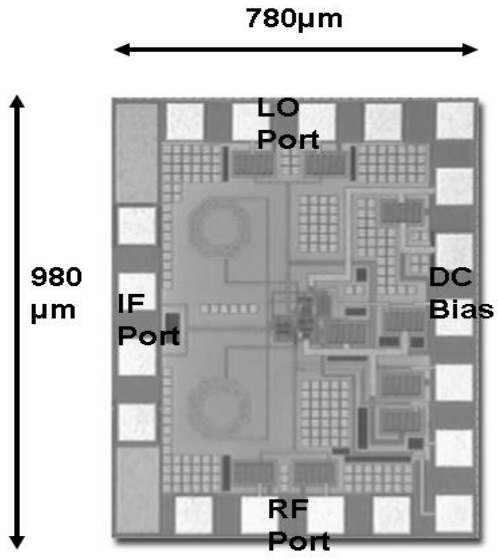


(b)



(c)

Figure 5.4 (a) Circuit diagram of the mixer with the static current bleeding and two resonating inductors (b) Small signal model (c) Simplified small signal model



(d)

Figure 5.4 Continued (d) Die photograph of the chip

Another important role of these two inductors is to protect RF current flowing into the current bleeding circuit. This helps RF current flow into the mixer output directly. Therefore we can achieve more conversion gain than the conventional current bleeding technique. As can be seen from Figure 5.4(b), LO drives node A and B in phase and a common mode equivalent circuit has been used for analyzing the circuit. If the RF transconductance stage works differentially, the node between L1 and L2 is virtually short as shown in Figure 5.4(b).

Figure 5.4(c) shows the simplified small-signal model of Figure 5.4(a) for half of the double-balanced mixer and same analytical method can be applied to the other half. The input impedance in the parallel RLC resonant circuit, shown in Figure 5.4(c), is

$$Z_{in} = \frac{1}{gm_1} \| \frac{1}{gm_2} \| \, j\omega L_1 \| \frac{1}{j\omega C_p} = \left((gm_1 + gm_2) + \frac{1}{j\omega L_1} + j\omega C_p \right)^{-1}, \tag{5.2}$$

and the power delivered to the resonator is

$$P_{in} = \frac{1}{2} Z_{in} \left| I_{RF} \right|^2 = \frac{1}{2} \left| I_{RF} \right|^2 \left((gm_1 + gm_2) + \frac{1}{j\omega L_1} + j\omega C_p \right)^{-1}. \tag{5.3}$$

The power dissipated by the resistors, $1/gm_1$ and $1/gm_2$, is

$$P_{\text{Res}} = \frac{1}{2} \frac{\left| V_{RF} \right|^2}{\dfrac{1}{gm_1 + gm_2}}, \tag{5.4}$$

the average magnetic and electric energy stored in the inductor, L_1, and in the tail capacitance, C_p, are

$$E_{L1} = \frac{1}{4} L_1 \left| I_{L1} \right|^2, \quad E_{Cp} = \frac{1}{4} C_p \left| V_{RF} \right|^2. \tag{5.5}$$

From (5.3) and (5.5),

$$Z_{in} = \frac{2P_{in}}{\left| I_{RF} \right|^2} = \frac{P_{Res} + 2\, j\omega (E_{L1} - E_{Cp})}{\left| I_{RF} \right|^2 / 2}. \tag{5.6}$$

At resonance when $E_{L1} = E_{Cp}$,

$$Z_{in} = \frac{P_{\text{Res}}}{\left| I_{RF} \right|^2 / 2} = \frac{1}{gm_1} \| \frac{1}{gm_2} = \frac{1}{gm_1 + gm_2}, \tag{5.7}$$

$$\omega_0 = \frac{1}{\sqrt{L_1 C_p}}, \; Q = \frac{1}{\omega_0 L_1 (gm_1 + gm_2)} = \frac{\omega_0 C_p}{gm_1 + gm_2}. \tag{5.8}$$

where ω_0 is the resonant frequency. From (5.7), the input impedance at resonant

frequency, ω_0, is a purely real impedance. By using two resonating inductors, we have decreased the effect of the tail capacitance, Cp. Therefore, as can be analyzed from (3.8) and (3.13), we have improved conversion gain by 6 dB and flicker corner frequency by 425 kHz in comparison to the Gilbert-type mixer based on the current bleeding technique.

B. Mixer Performance Summary

By using the Gilbert-type mixer with the static current bleeding technique and two resonating inductor, a measured conversion gain of 16dB and a flicker corner frequency of 125kHz has been achieved. The flicker corner frequency has been improved by 775kHz compared to the conventional Gilbert-type mixer. Detailed measurement results are compared and summarized in Section 5.4.

5.2 Design consideration for low flicker noise VCO

In general, the mixer is the main source of flicker noise in a receiver system and as shown in (5.9), flicker noise by the direct mechanism is inversely proportional to the product of the slope of the LO waveform at zero-crossing and its period. The signal-to-noise-ratio (SNR) for direct noise and indirect noise is given by respectively [5]

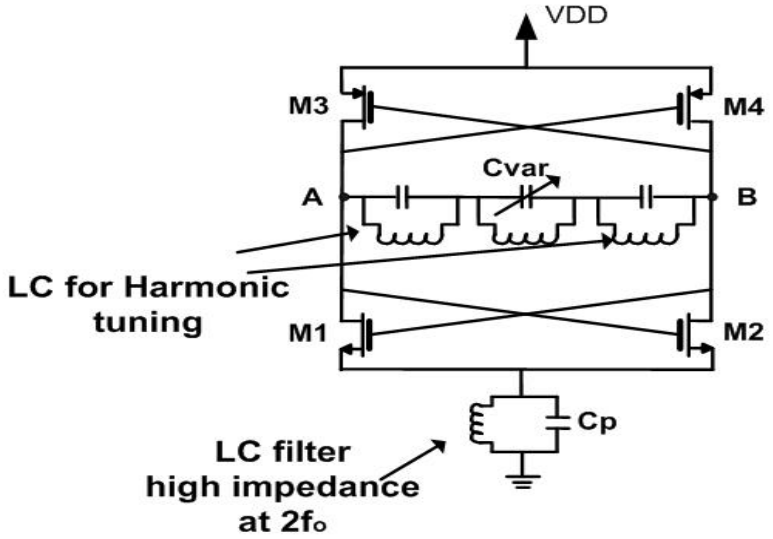
$$SNR_{dir} = \frac{S \times T}{2\pi(V_{GS} - V_t)} \bullet \frac{V_{in}}{V_n} \tag{5.9}$$

$$SNR_{ind} = \frac{g_m \frac{2}{\pi}}{2 f_{LO} C_p} \bullet \frac{V_{in}}{V_n} = 2 \frac{f_T}{f_{LO}} \bullet \frac{V_{in}}{V_n}$$

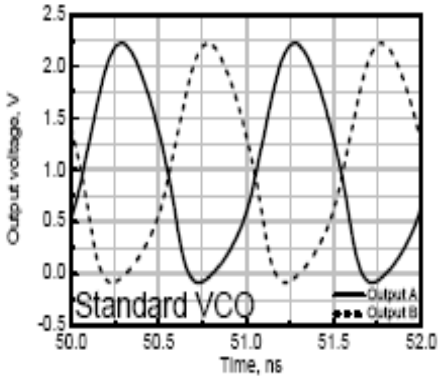
(5.10)

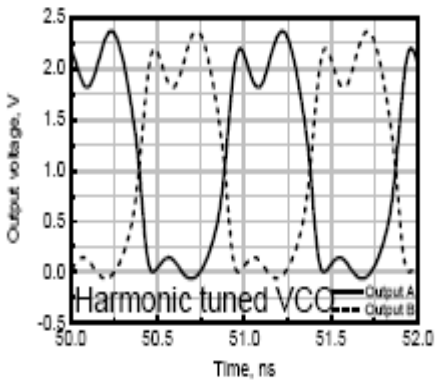
where S is the slope of the LO waveform, T is the period of the LO waveform, Cp is the tail capacitance of the source node for LO. From (5.9), flicker noise by direct mechanism at the mixer output may be deleted if the LO waveform is a perfect square-wave with infinite slope at zero-crossing. Also, from (5.10) the effect of flicker noise can be reduced by minimizing the tail capacitance, or equivalently, increasing the unity current gain frequency of the transistors (f_T). Therefore, a method to generate a LO waveform which has sharp transitions at zero-crossing is proposed by using a harmonic-tuning VCO. As can be seen from Figure 5.5(a), between the node A and B, two more LC tanks are connected to the original LC tank of VCO. The additional LC tanks are open at the fundamental and third harmonic frequency and short at the second harmonic frequency. The inductor connected to the source of M1 and M2 to resonate the tail capacitance, Cp, roles as a noise filter with the tail capacitance. It prohibits the resonator being loaded by

differential pairs (M1 and M2) in triode region and then it helps protect the resonator from reducing the quality factor (Q) [22]. The harmonic tuning and noise filtering techniques were proposed to improve the phase noise performance of VCO [22]-[23]. In this proposal, the harmonic tuning technique for VCO is proposed to make a fast-transiting LO waveform that is used as an LO input to the mixer. By simulation results, as can be seen in Figure 5.5(b) and (c), the slope of LO waveform using the harmonic tuning technique is much faster than the standard one.



(a)



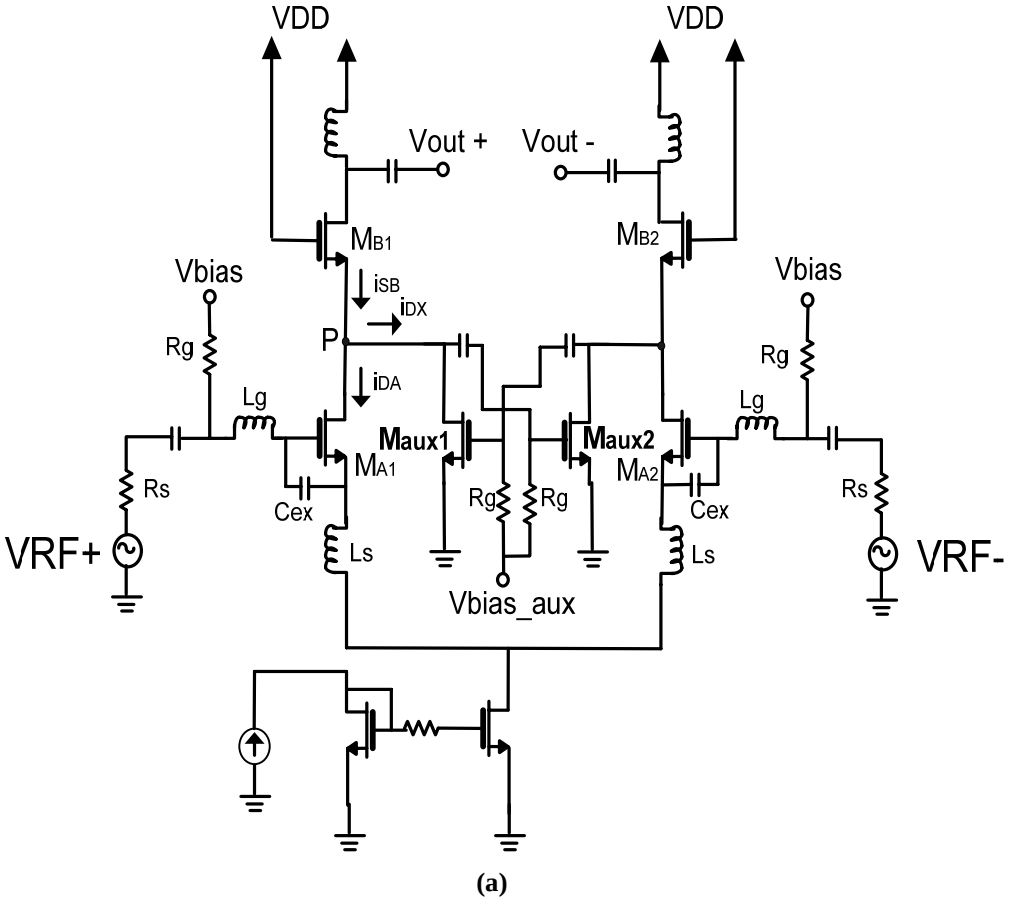


(b) **(c)**

Figure 5.5 (a) Proposed VCO (b) Waveform of the standard VCO (c) Waveform of the harmonic tuned VCO

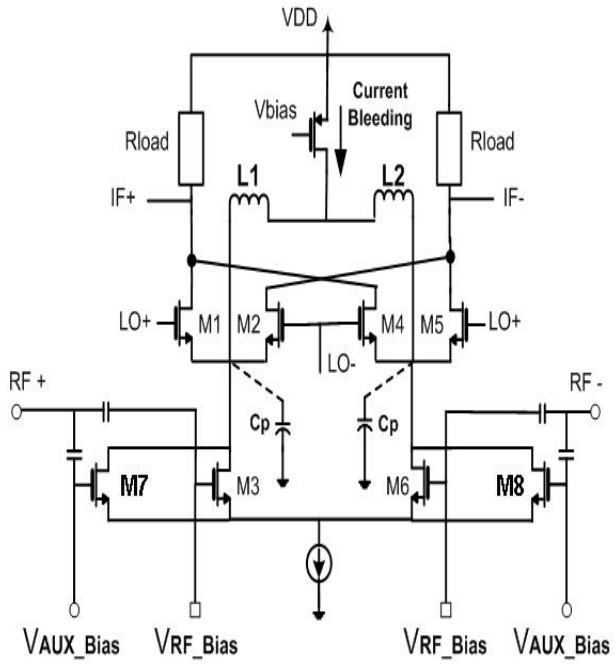
5.3 Design consideration for low flicker noise receiver front-end

To implement a low flicker noise receiver front-end, a differential LNA which was used in Chapter IV and low flicker-noise mixers have been designed and measured. Mixer has to have excellent flicker-noise performance. A differential LNA does not contribute any flicker noise to the receiver system and a mixer is the main contributor of whole flicker noise performance in receiver front-end.

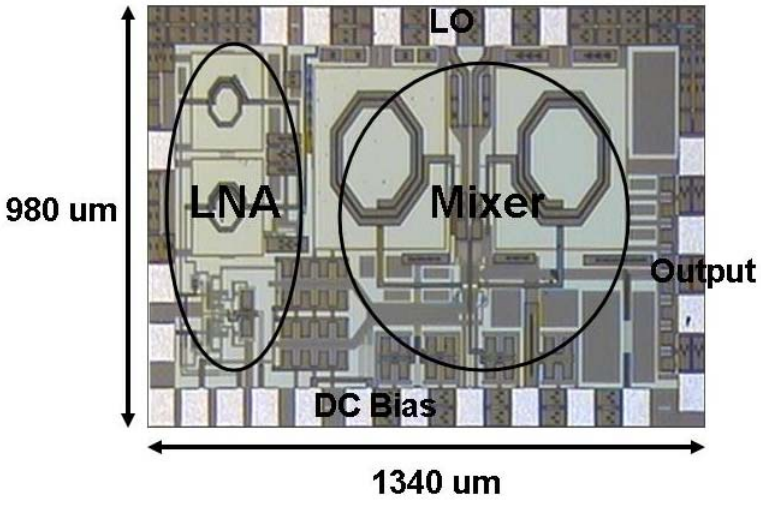


(a)

Figure 5.6 (a) Differential LNA



(b)



(c)

Figure 5.6 Continued (b) Low flicker-noise mixer (C) Die photograph of the receiver front-end

5.4. Measurement results

The chip microphotographs of the three mixers are shown in Figure 5.2(c), Figure 5.3(d), and Figure 5.4(d). For comparison purposes, a conventional Gilbert-type mixer has also been fabricated. The conventional Gilbert-type mixer was designed exactly the same as the mixer with the current bleeding technique as shown in Figure 5.2(a) except the current bleeding circuit. Figure 5.3(d) is the die photo of the Gilbert-type mixer with the current bleeding and one resonating inductor and Figure 5.4(d) is the die photo of the mixer with two resonating inductors.

All measurements were performed using an on-wafer probe station. Table 5.1 summarizes the measured results for the four fabricated mixers and shows that the proposed two mixers using the resonating technique outperform the conventional current bleeding mixer on conversion gain and flicker corner frequency.

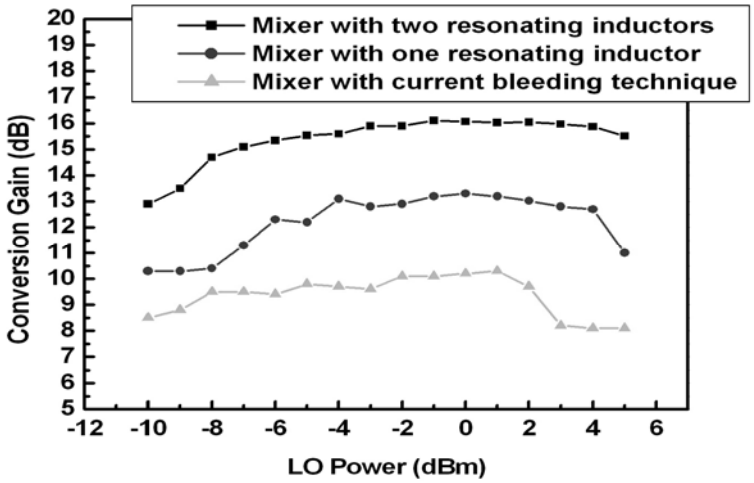


Figure 5.7 Measured conversion gain variation with LO power

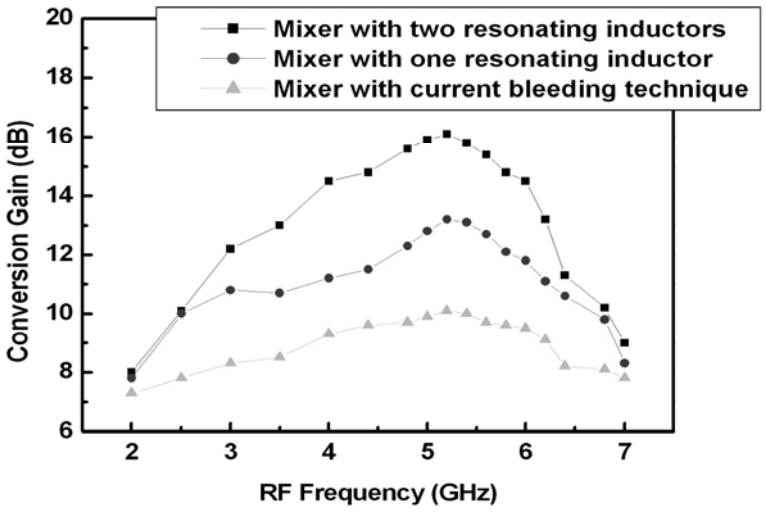


Figure 5.8 Measured conversion gain variation with RF frequency

It also shows that the proposed mixer based on the current bleeding technique with two resonating inductors has the best performance on conversion gain and flicker corner frequency. The variations of conversion gain with LO power for all three mixers were measured and are plotted in Figure 5.7. In Figure 5.8, conversion gain is decreased as the resonating frequency is changed, especially for two mixers: the mixer with one resonating inductor and the mixer with two resonating inductors. This means that conversion gain is maximized under resonant condition for these two mixers as we analyzed in Section 5.1.

Table 5.1 Measured results of four mixers

Topology	IDC (mA)	IIP3 (dBm)	**Conv. Gain (dB)**	**Flicker Corner Freq. (kHz)**
Gilbert-type Mixer	3.9	-5.5	**9**	**900**
Mixer with current bleeding only	3.9	-5.2	**10**	**550**
Mixer with current bleeding and one inductor	3.9	-5.2	**13**	**180**
Mixer with current bleeding and two inductors	3.9	-5	**16**	**125**

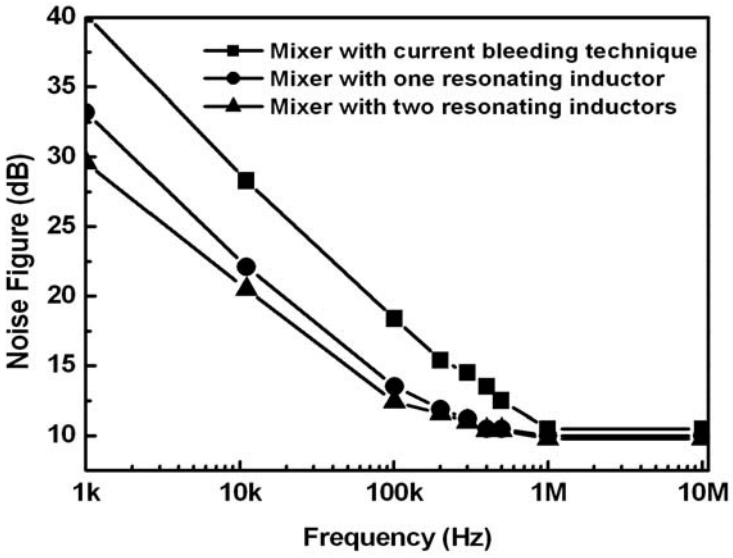


Figure 5.9 Measured noise figures of the three mixers

Figure 5.9 shows the measured noise figures for three mixers and more detailed results are summarized in Table 5.3. Also, the noise figure of the mixer with two resonating inductors is found to be 9.8 dB at 1 MHz and above. At the rated RF frequency of 5.2 GHz, the measured conversion gain for the mixer with two resonating inductors is 16.2 dB and this gain is obtained when the balanced LO signal powers are at -1 dBm. The mixer has a measured input 1dB compression point of -14 dBm and an IIP3 of -5 dBm as shown in Figure 5.10 and Figure 5.11, respectively. The LO to RF isolation is 36.3 dB. Figure 5.12 shows output noise power spectral density which was measured on both HP 4395A Low-frequency Spectrum Analyzer and Agilent 35670A Dynamic Signal Analyzer for more accurate measurement. The measured flicker noise corner frequency is 125 kHz which is the lowest corner frequency ever reported using a CMOS active mixer with a more than 15 dB of conversion gain based on experimental results. Also, the variations of the flicker corner frequency with the four different bleeding currents were measured for the mixer with two resonating inductors and summarized in Table 5.2.

As we increase the bleeding current, the bias current of the LO switches is decreased and simultaneously the noise current generated by the direct mechanism is also decreased. Therefore, as we analyzed in Section 3, the flicker corner frequency is decreased. The noise figure of the mixer with two resonating inductors was measured and plotted in Figure 5.13. Table 5.4 summarizes the measured flicker corner frequency of the low flicker-noise receiver front-end which is shown in Figure 5.6(c).

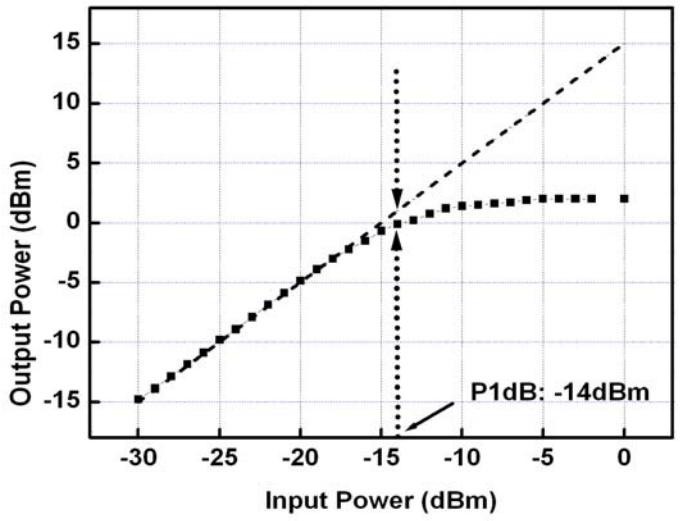


Figure 5.10 Measured input 1-dB compression point of the mixer with two resonating inductors

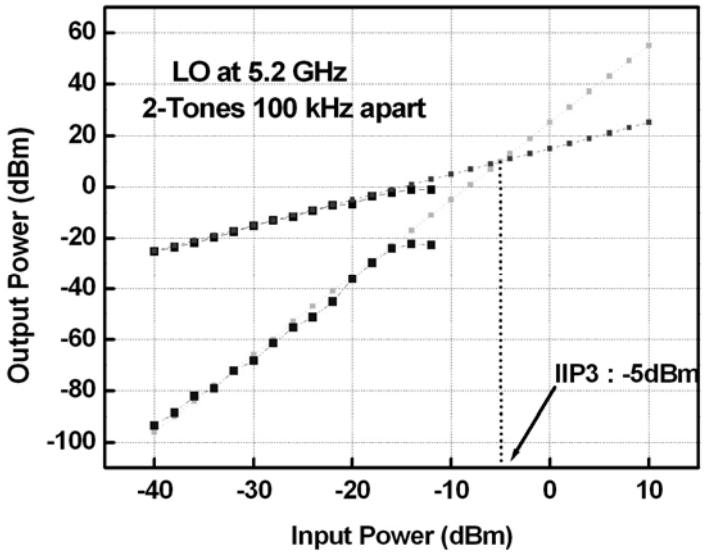


Figure 5.11 Measured Input third order intercept point of the mixer with two resonating inductors

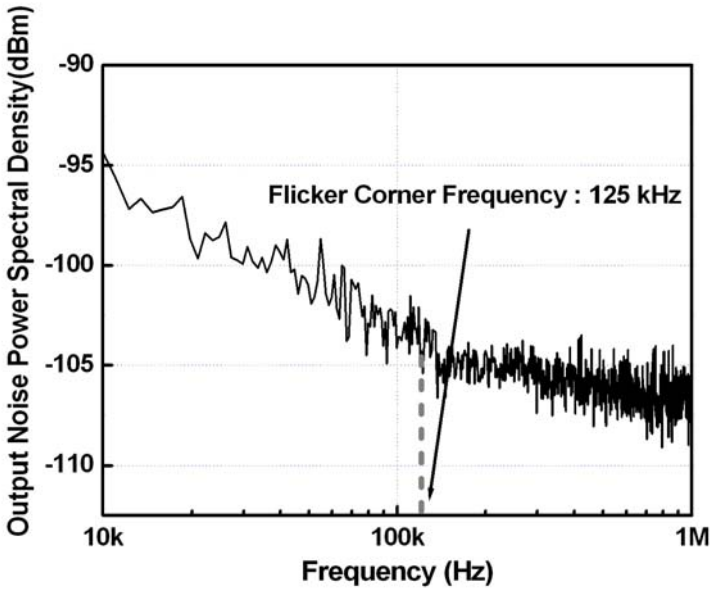


Figure 5.12 Measured flicker corner frequency of the mixer with two resonating inductors

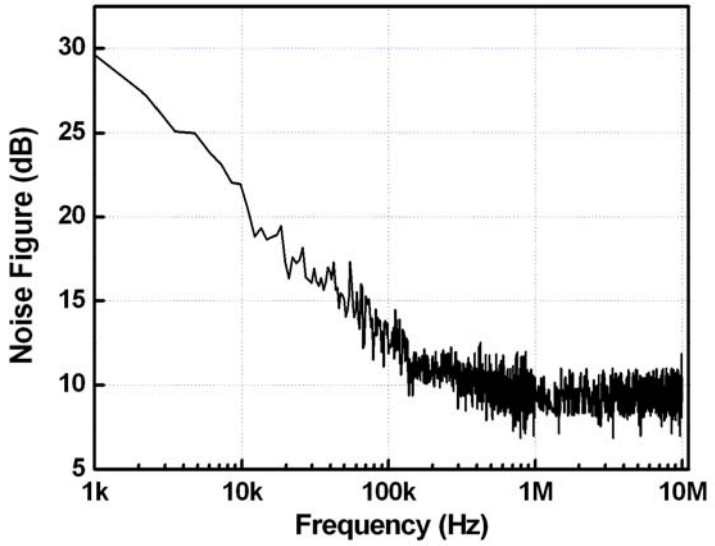


Figure 5.13 Measured noise figure of the mixer with two resonating inductors

Table 5.2 Measured results of flicker corner frequency with bleeding current variations

IDC (mA)	Bleeding Current (mA)	LO Switches Current (uA)	**Flicker Corner Freq. (kHz)**
3.9	3.85	**50**	**125**
3.9	3.8	**100**	**170**
3.9	3.75	**150**	**230**
3.9	3.7	**200**	**305**

Table 5.3 Comparison of mixers

Topology	**Gain**	**IIP3**	**Noise Figure**	**Flicker Corner Freq.**	**Power**	**RF Frequency**	**Technology**
Static Bleeding[4]	13dB	-10.6dBm	27dB	NA	5.16mW	900MHz	0.35um CMOS
Dynamic Bleeding[21]	0dB	10.5dBm	11dB	10kHz	2.4mW	2GHz	0.13um CMOS
Mixer with LC filter[24]	44dB with Receiver	-2dBm	6.2dB with Receiver	350kHz	7.2mW	2.1GHz	0.18um CMOS
Passive Mixer[25]	26dB with LNA	5dBm	3.5dB with Receiver	200kHz	72mW for Receiver	5GHz	0.18um CMOS
Gilbert Mixer with current bleeding	10dB	-5.2dBm	10.5dB	550kHz	7mW	5.2GHz	0.18um CMOS
Gilbert Mixer with current bleeding and one inductor	13dB	-5.2dBm	10dB	180kHz	7mW	5.2GHz	0.18um CMOS
Gilbert Mixer with current bleeding and two inductors	16dB	-5dBm	9.8dB	**125kHz**	7mW	5.2GHz	0.18um CMOS

Table 5.4 Measured results of flicker corner frequency of receiver front-end

Topology	IDC (mA)	**IIP2 (dBm)**	**IIP3 (dBm)**	**Flicker Corner Freq. (kHz)**
Conventional receiver front-end	10	35	0	900
Low flicker-noise receiver front-end	9	**45**	**5**	**135**

CHAPTER VI

Conclusion and Future Works

6.1 Technical contributions and impact of the dissertation

The direct conversion receiver (DCR) architecture has gained considerable attention so far because it reduces the need for filters and other external components, which enables a higher level of integration than super-heterodyne architectures. Two major issues, the linearity and flicker noise, are discussed in this research. The objective of research in this dissertation is to develop techniques to achieve a highly linear and low-flicker noise receiver front-end which consists of a highly linear LNA, a highly linear and low-flicker noise mixer, and a harmonic tuned VCO in CMOS technology for C-band application.

Some design techniques to make a highly linear LNA, a highly linear mixer, and a low flicker-noise mixer are proposed. As seen in the preliminary research contributions, the Gilbert-type mixer with the static current bleeding and two resonating inductors provide promising solutions to achieve low-flicker noise direct conversion receiver. Simultaneously, additional techniques are required to improve the linearity performance of LNA and mixer.

The research in this dissertation has focused on enhancing the linearity of LNA and mixer to improve the total linearity of the receiver on one hand, and on improving the flicker-noise performance of the receiver on the other.

To implement a low flicker-noise receiver front-end, three double-balanced Gilbert-type down conversion mixers, i.e., a Gilbert-type mixer based on the current bleeding technique, a Gilbert-type mixer based on the current bleeding technique with one resonating inductor, and a Gilbert-type mixer based on the current bleeding technique with two resonating inductors, have been designed and analyzed to improve flicker noise performance without sacrificing conversion gain, NF, and linearity performance for direct conversion receivers. Also, a conventional Gilbert-type mixer has been fabricated and measured for comparison purposes. The proposed mixers, fabricated in a 0.18 um CMOS process, show significantly improved performances on flicker noise, conversion gain. The main ideas of the proposed mixers are to reduce the bias current of LO switches, to resonate the tail capacitance (Cp), and to minimize the amount of RF current flowing into the current bleeding circuit. Among the three CMOS mixers, the Gilbert-type mixer based on the current bleeding technique with two resonating inductors shows the best performance on flicker noise and conversion gain. In this mixer, two inductors are separately connected to each node between the current bleeding PMOS device and LO switching devices in order to resonate the tail capacitance out. In addition, the inductors protect RF current flowing into the current bleeding circuit, which results in improvements of conversion gain. By using two inductors, conversion gain is increased by 6 dB in comparison to the Gilbert-type mixer based on the current bleeding technique and the flicker corner frequency is decreased from 550 kHz to 125 kHz which is the

lowest flicker corner frequency ever reported among CMOS active mixers with more than 15 dB of conversion gain. In conclusion, the Gilbert-type mixer based on the current bleeding technique with two resonating inductors shows better results on flicker noise and conversion gain performance than the other two mixers. Also, simulation results using a harmonic tuned VCO have been shown to improve the total flicker noise performance of receiver front-end and we have proved that the effect from VCO part is not critical.

To implement a highly linear receiver front-end, a differential LNA using IMD sinking method and two Gilbert-type mixers using DS technique (one with separate RF bias voltage and the other one with grounded RF bias voltage) with two resonating inductors. The mixer using grounded RF bias voltage with two resonation inductors has a measured input 1dB compression point of -6 dBm and an IIP3 of 15.3 dBm which is the highest IIP3 value ever reported using a CMOS active mixer based on experimental results.

6.2 Scope of future research

In this dissertation, research has focused on the implementation of a highly linear and low flicker-noise receiver front-end for multiband direct conversion architecture. A highly linear differential LNA using IMD sinking method has been demonstrated to generate differential signals for the RF inputs. The design can be simplified by using a single-ended version using an active balun. Also, other linearization techniques to make a highly linear LNA can be applied for multiband applications and it would be a very challenging task. Even though we have achieved a highly linear and low flicker-noise

mixer, more challenges remain for the quadrature modulation and flicker noise optimization by doing theoretical understanding from VCO part. Two more general problems in implementing direct conversion receivers are dc-offset and I/Q imbalance. For dc-offset problem, a highly linear LNA and mixer based on low flicker-noise performance should be designed with additional dc-offset circuitry like auto-zeroing and chopping technique. For I/Q imbalance, additional circuitry can be added to receiver front-end or DSP algorithms at the baseband can be very helpful.

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Vita

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